AME 463 – Finite Element Analysis

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Final Project Part 5: Finite Element Analysis of Nvidia Jetson Thor Chip

Summary of Project parts 1-4:

This project focuses on modeling the thermal behavior of an Nvidia Jetson Thor chip using ANSYS. In previous parts of the project, a simplified model of the chip was created using SpaceClaim (Figure 1), which shows the chip as a stack of seven rectangular prisms consisting of the PCB, BGA, package substrate, RDL, device layer, die, and TIM. Each layer was assigned material properties based on provided thermal conductivities (Table 1), and realistic boundary conditions were applied to simulate natural cooling by convection.

Power maps were introduced to represent heat generation across the device layer, and steady-state thermal simulations were performed to analyze temperature distributions throughout the chip (Figure 2) [1]. These results showed expected behavior, with the highest temperature reaching 89.789° C near the heat-generating regions and the greatest cooling effects through the TIM and PCB layers, with a minimum temperature of 72.239° C as seen in Figure 3 [2].

A convergence study was conducted on elements ranging from 12 to 0.125 mm, successively halving element size and recording temperatures and computation times across each face. The goal was to ensure that the results are not dependent on mesh size. Convergence was assessed using a percent difference in probe temperature between successive meshes as seen in Table 2 [3]. We found that a 0.5 mm mesh provided a good balance between computation time and convergence, with the average difference across each layer being 0.3%.

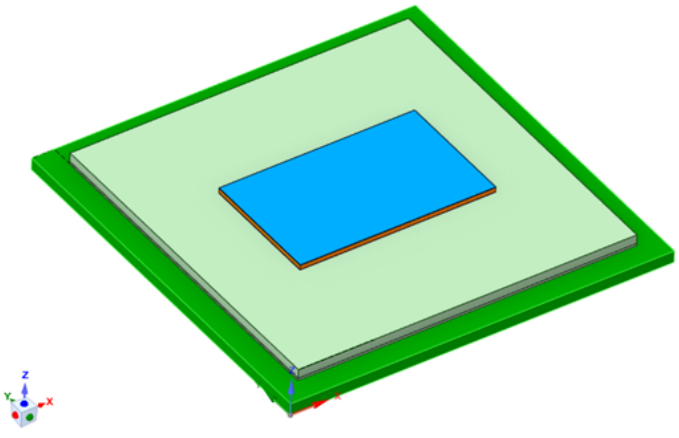


Figure 1: CAD model of the Nvidia Jetson Thor Chip

Material	Thickness (μm)	Young's Modulus (Gpa)	Poisson's Ratio	Thermal Conductivity (W/mK) (x,y,z)	Coefficient of Thermal Expansion (ppm/k) (x,y,z)
PCB	1570	21	0.29	30,30,3	16,16,60

BGA	300	35	0.35	0.3,0.3,20	22
package substrate	1200	20	0.4	70,70,7	15,15,55
RDL	50	25	0.33	2, 2, 25	30
DIE	600	150	0.27	149 (at 25 °C), 110 (at 100 °C)	2.8
TIM	50	0.005	0.48	2.9	100

Table 1: Thermal conductivities for each chip layer [4]

Thermo-Mechanical Study (Project Part 5):

Thus far, we have seen the impact that different loads have on the chip's thermal performance. In this final section of the project, we aimed to investigate the effect that this thermal load, in turn, has on the physical structure of the stack. That is to say, we want to find what stresses are created by the heat generated in the chip due to differences in the thermal expansion coefficients in each layer, as seen in Table 1. We will break this project section into 6 main tasks.

Mechanical Boundary Conditions:

To start, a static-structural analysis system was added to ANSYS Workbench alongside the existing steady-state thermal block from part 4 of the project. The model of the thermal system was then linked to the model of the static structural system. The thermal system solution was also linked to the setup of the static structural system. The coefficients of thermal expansion from Table 1 for each layer material were added to the engineering data as well. Next, the structural setup was opened in ANSYS Mechanical.

Within Mechanical, we needed to set appropriate boundary conditions for our structural analysis. It's worth noting that since we imported the solution from the thermal analysis, that means that we are using the same thermal boundary conditions that we applied in part 2 of the project. That being a convective boundary layer of 5,000 W/m^2K applied to the top surface of the TIM layer, and a 20 W/m^2K convective boundary layer being applied to all other exposed surfaces. For the static solution, we only applied one boundary condition. A "fixed support" was placed on the bottom surface of the PCB.

This single boundary condition is sufficient to prevent rigid body motion because it prevents movement in all 6 degrees of freedom. Further, the fixed support may introduce some artificial stiffness, but we are still not over-constraining the model, as our boundary condition is a reasonable approximation since the PCB would be constrained by a much larger structure in reality.. The physical justification for this is that in our model, the PCB layer is only shown to be a 51 x 51 mm square, but in the real world, the PCB would likely be much larger. If this Nvidia Jetson Thor chip were placed on a graphics card, for example, then the PCB would be several inches longer in each dimension, and would be physically attached to the larger structure of the computer. This means that we can use the PCB as a reference point and assume that it does not move in space.

Strain Analysis:

Now that we have our boundary conditions set, the solution can be solved in ANSYS to obtain our desired strain results. This is done by inserting multiple items under the solution folder in ANSYS. We are interested in two shear strains: γ_{xz} and γ_{yz}, where z is in the thickness direction. We ran this simulation using Power Map 1 provided by the course site [4]. We created contour plots on the top surface of every device layer for each of these stresses. To expedite the process, we injected a Python script into ANSYS Mechanical to automatically take a screenshot on each result [5]. The plots can both be seen in Table 3. [6].

Looking at our results, we see that the strain plots for each device layer are very similar in shape. Each of the plots shows a linear relationship across the layer, with maximum values being along the outer edges of the chip (and on contact edges between the package substrate and RDL). For the γ_{xz} strains, the strain values are varied along the X axis, and the values are varied along the Y axis for the γ_{yz} strains. Note that shear strain is zero in the center of the chip for every layer. This is also due to the symmetry of the chip, where the forces seen from the layers pull equally in opposite directions in the center region. The magnitude of strain varies across different device layers, with some having larger values than others. This makes sense as the strain largely comes from the difference in thermal expansion coefficient between different layers. So, contact surfaces between two layers with large differences in thermal expansion will have a higher magnitude of strain.

Mesh Quality & Refinement:

As mentioned in the previous project part, we conducted a mesh independence test to ensure that our solution converged for the steady state thermal analysis. Since the selected mesh size of 0.5 mm was proven to converge for the thermal analysis, it follows that the solution would also be convergent for our static structural analysis. And as we can see from Table 3, this assumption holds [6]. We can see that regardless of stress type or device layer, there are no distorted or poorly shaped elements in our solution. This is even true in the thin and mechanically weaker layers (the TIM and RDL). For the sake of comparison, we re-ran the simulation with a much larger element size of 6 mm. As an example, Figure 2 shows the maximum principal stress on the PCB.

The smaller element size results in a very poor mesh. All of the elements are distorted, especially the elements on the exterior edges of the model. This shows that our earlier convergence testing was valuable, as the simulation with the larger element size clearly does not have converging results. The stress is concentrated in different areas of the PCB, as well as being different in magnitude. This is all clearly a result of the distorted elements.

In some situations, this distortion could be remedied in multiple ways, such as using tetrahedral elements or local refinement of the mesh in areas with high distortion. However, in our case, we find that it is more than sufficient to simply use a smaller element size. Again, this is clear as our 0.5 mm mesh showed no perceivable distortion whatsoever.

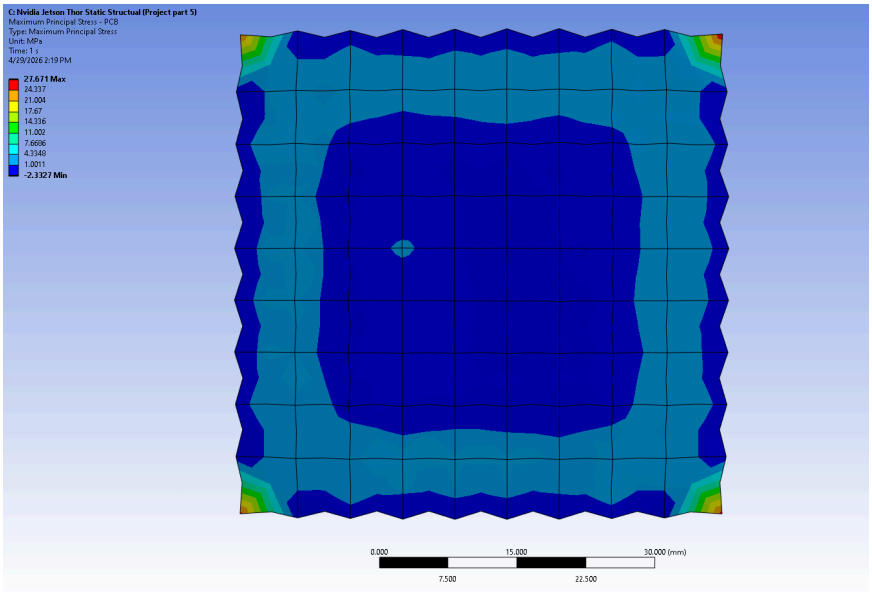


Figure 2: Maximum principal stress on PCB for power map 1 using 6 mm elements

Stress Analysis:

With our mesh quality being confirmed, we will now measure various stresses across the chip layers. Again, we will add several items to the results section in ANSYS Mechanical. For power map 1, we captured normal stress in the Z direction, shear stress in the XZ and YZ directions, maximum and minimum principal stresses, as well as the maximum shear stress. Again, we created contour plots scoped to the top surface of each layer using the previously mentioned Python script [5]. The plots are shown in Table 4 [7].

As we can see from the stress contours, each of these stresses behaves differently from one another and across device layers. In general, we see that stresses are smaller in magnitude in the PCB, BGA, and package substrate than in the RDL, Die, and TIM. This makes sense as the larger layers are cooler than the smaller ones and thus experience less thermal expansion. The stresses also have a larger area to be spread over in the PCB, BGA, and package substrate.

However, we also see that for the same given stress type, the behavior is consistent across layers. Take the XZ and YZ shears, for example. We can see that just like with shear strain, the shear stress forms a linear relationship across either the X or Y axis, regardless of device layer, and the shear is always zero in the center of the chip. Shear stresses are seen as concentrations at the edges where layers connect. This makes sense as geometric edges of interfaces typically see localized stress intensification.

While shear stress shows a linear relationship on every layer, normal stress is much more dependent on the powermap and its subsequent concentrations in temperature. We can see in each layer that the normal stress is of a far higher magnitude in areas that have a higher temperature, especially on the RDL, which is where the power map's heat flux was applied. The main stress concentration mechanism here comes from the differences in thermal expansion coefficients across device layers. Each layer will expand a different amount due to the same given temperature. Since the layers are bonded

together, they instead develop stresses. This is the same mechanism behind the movement of bimetallic strips such as those found in household thermostats. Similarly, the mismatch of elastic modulus between each layer also causes stress concentrations at layer interfaces as stiffer materials resist deformation, but deformation is continuous throughout the chip. Ultimately, this means that throughout the chip, we see the highest stresses at interfaces where the two layers have the largest difference in thermal expansion coefficients and stiffness, such as between the RDL and DIE.

Correlation Between Maximum Shear Stress and Temperature:

Now that we have stress distributions for each layer and confirmed the validity of our mesh, we can compare our results to the temperature map of each layer that was obtained in part 2 of this project. The temperature distributions were found in previous project parts and are shown in Table 5 [8]. In comparing our results across each device layer, we can see that on some layers, there is a small positive correlation between high temperatures and regions of high shear. However, this correlation is somewhat weak and is not seen on every device layer.

Take, for example, the PCB. The color gradients have almost no correlation. The temperature map shows a round hotspot near the center of the PCB, whereas the maximum shear plot is constant in this region with a square shape. Only the corners match in relative magnitude. The RDL, on the other hand, shows a very strong correlation between the temperature and maximum shear strain. The shapes and hot spots of both plots almost perfectly match. The TIM also shows a strong correlation. The package substrate shows a positive correlation, but only at the interface to the RDL. The BGA shows a small correlation, but this is vague. Lastly, the top surface of the DIE shows no correlation at all.

This behavior may seem strange at first, but this is actually what we should expect. Recall the formula for thermal strain: $\varepsilon=\alpha\Delta T$. Here we see that strain is equal to the coefficient of thermal expansion times the difference in temperature. This means that strain is highly dependent on the difference between the thermal expansion coefficients at the interface of each layer. Again, our results in ANSYS were all placed on the top layer of the respective layer. So when we look at the results for the RDL, for example, we are looking at the cross-section of the chip where the RDL meets the layer directly above it (the Die). This means that only layers with a large difference in thermal expansion will show a correlation between temperature and maximum shear, which is exactly what we see. The PCB, BGA, and package substrate only show small correlations because the difference in thermal expansion at their respective interfaces is small. The RDL shows a strong correlation because it has a thermal expansion coefficient of 30 ppm/k and the die above it has that of only 2.8 ppm/k.

However, there is one exception to this. We do not see a correlation at the interface between the Die and TIM, despite the fact that this layer has the largest difference in thermal expansion coefficients. This is because the TIM is made of a very soft material, meaning that the difference in Young's modulus results in more deformation and less stress. The Die has a Young's modulus of 150 GPa, whereas the TIM's modulus is only 0.005 GPa. This stiff-soft interface causes a lack of correlation between the temperature and shear stress at this location.

Multiple Power Maps:

All of the above steps were repeated for powermaps 2 and 3. The stress and strain contours for these powermaps are shown in tables 6 through 9 [9-12]. Largely, the shapes of the contours do not change across powermaps, at least visually. Maximum temperature does change location as shown in previous parts of this project, but that is the biggest change, as the power map directly correlates with imported heat flux.

Most importantly, we can see that our analysis thus far is consistent across different power maps. For example, the linear behavior we see with the XY and ZY stresses and strains is consistent. As is the fact that only some layers show a correlation between maximum shear stress and temperature. The same layers that show correlations are consistent across all three power maps. Furthermore, the location of stress and strain concentrations is consistent. Applying different power maps does not largely change the location of the maximum stress or strain, except when looking at temperature-dependent stresses.

We even see that the magnitudes of some stresses stay similar across different powermaps. Take, for example, the maximum shear stress as seen on the top surface of the Die. On PowerMap 2, the highest magnitude of the max shear stress is 10.688 MPa. For PowerMap 3, the same quantity is 10.985 MPa. This shows that the interfacial shear stresses have a low sensitivity ot power distribution, at least in terms of magnitude.

Bonus Study:

As a bonus study, we analyzed a chip with two additional layers: Micro-bumps placed in between the Die and RDL, and C4 bumps placed between the RDL and package substrate. The properties of these two layers are shown below:

Material	Thickness (μm)	Young's Modulus (Gpa)	Poisson's Ratio	Thermal Conductivity (W/mK)	Coefficient of Thermal Expansion (ppm/k)
Micro-bumps	15	60	0.35	21	35
C4 Bumps	70	40	0.35	35	22

Table 10: Material properties for Micro-bumps and C4 bumps

Both of these materials represent tiny balls of solder that serve as electrical interconnects between layers. The previous tasks were repeated with the addition of these layers, using only power map 1. The resulting stress and strain contours are shown in Tables 11 and 12 [13-14]. First, let's compare the results for γ_{xz} and γ_{yz} strains. We still see the aforementioned linear relationship on the two new layers. We can see that the magnitudes of some strains change, however. For example, the XZ shear strain seen on the die increased slightly from 1.5667×10^{-5} to 1.9768×10^{-5} mm/mm. Similarly, the YZ shear strain seen on the RDL increased from 0.0010627 to 0.0023746 mm/mm at maximum. While these values are small, the increase is roughly double. This makes sense as introducing the new layers changes the load-transfer path but does not necessarily move the global regions where shear is highest. The bump layers increase the strain magnitude because the load transfer becomes more localized and more compliant.

We also see that our mesh quality is still sufficient with the new layers and needs no refinement, just as before. Again, this makes sense as we have already conducted a mesh independence study. The introduction of the microlayers could reasonably cause issues, as these layers are very thin, but our small mesh size is still sufficient.

As for the stresses, we see that for the larger layers (PCB, BGA, and package substrate) the stress does not change much in shape or location. The color gradients largely show the same shape, but again, the magnitudes are slightly higher. For example, the maximum shear stress on the BGA increased from 21.425 to 31.349 MPa. However, on the smaller layers (RDL, Die, and TIM), the shapes of the contours change. For example, the RDL no longer shows a correlation between temperature and normal stress with the addition of the bump layers. This is expected as the new layers introduce compliance between the existing chip layers, reducing the through-thickness restraint on the RDL. As a result, the normal stress becomes smaller in magnitude and much more uniform, while edge locations remain as dominant stress regions.

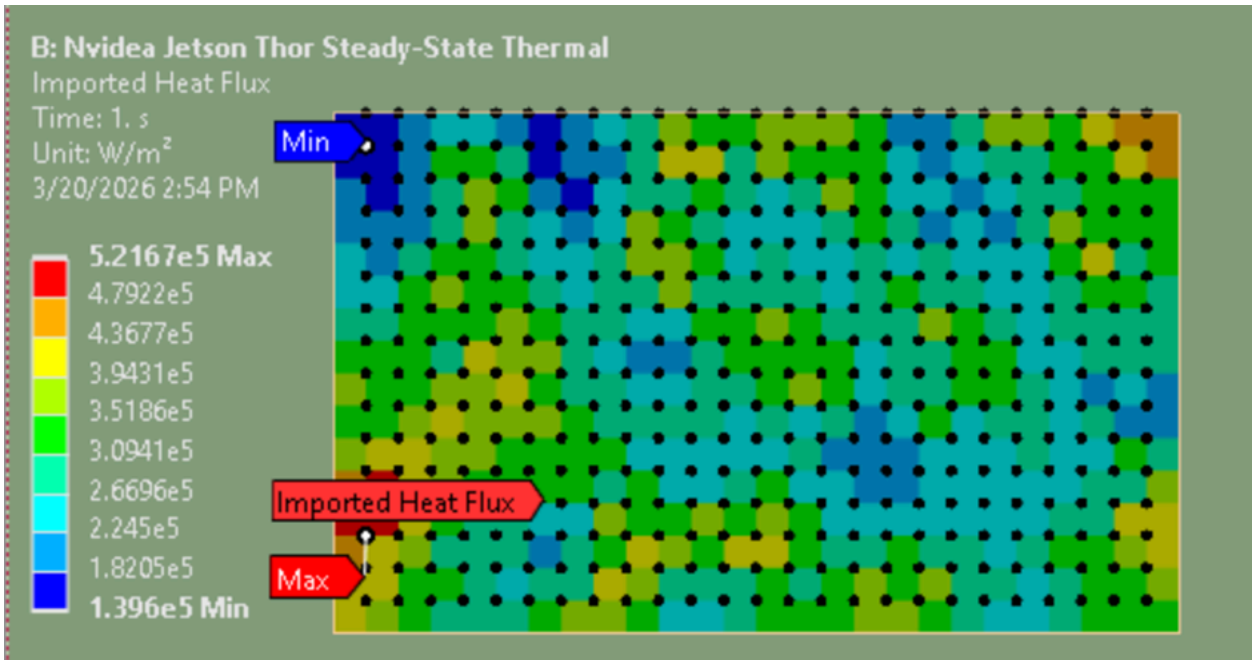
Adding the bumps does not affect the correlation between maximum shear stress and chip temperature. We still see the same behavior where some layers and stresses show a strong correlation, and others do not. This follows from our previous explanation of the difference in coefficients of thermal expansion. Again, we see a strong correlation on the TIM and RDL layers, and weak to no correlation on the other layers. Additionally, we also see that both bump layers show a strong correlation between temperature and maximum shear stress. This is consistent with our previous results, but it also suggests that the thickness of the layer contributes to this correlation. This is likely because thinner layers tend to have larger temperature gradients and less ability to redistribute strain throughout the layer, meaning the thermal expansion mismatch has a stronger effect on these layers.

Summary:

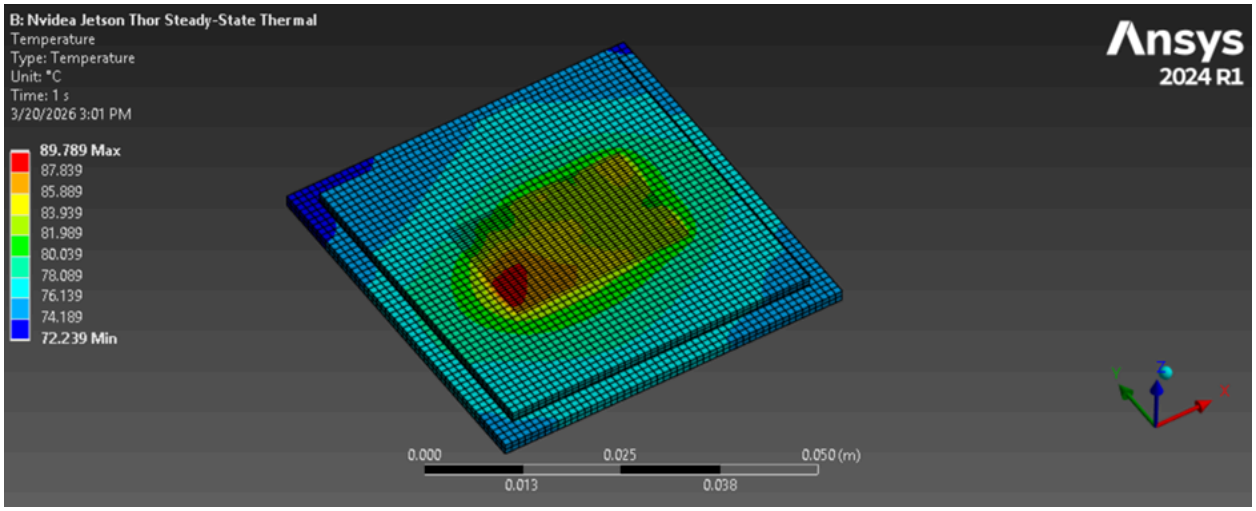
This project modeled the thermal and thermo-mechanical behavior of a multilayer Nvidia Jetson Thor chip using ANSYS, progressing from steady-state thermal analysis to structural stress and strain evaluation. Results showed that temperature distributions are governed by power input and cooling paths, while stresses and strains are primarily driven by mismatches in coefficients of thermal expansion and material stiffness between layers, leading to peak values at interfaces and edges. This leads to only certain device layers showing a strong correlation between temperature and maximum shear stress. We also showed that the addition of bump layers would introduce compliance that reduces through-thickness normal stresses and increases shear strain magnitudes, while preserving the overall deformation patterns and stress concentration locations.

Works Cited & Appendix

[1] Figure 2: Power map 2 after being imported into ANSYS as a Heat Flux:



[2] Figure 3: Generated Finite Element mesh showing steady-state temperature across the chip stack:



[3] Table 2: Percent change in computation time and peak layer temperature from previous element size:

Element size (mm)	ΔCP Time (m)	Δ PCB (C)	Δ BGA (C)	Δ Substrate (C)	Δ RDL (C)	Δ Die (C)	Δ TIM (C)	Δ Average (C)
8.000	19.62%	0.87%	1.47%	0.55%	2.35%	2.42%	2.36%	1.66%

4.000	28.10%	3.00%	3.27%	6.89%	5.45%	5.05%	4.94%	4.79%
2.000	271.43%	3.01%	3.01%	0.33%	0.11%	0.03%	0.03%	0.94%
1.000	7.39%	1.18%	1.19%	0.94%	1.17%	1.21%	1.18%	1.14%
0.500	295.40%	0.09%	0.09%	0.48%	0.44%	0.35%	0.35%	0.30%
0.250	503.91%	0.02%	0.02%	0.04%	0.08%	0.03%	0.03%	0.02%
0.125	1072.37%	0.06%	0.06%	0.07%	0.07%	0.05%	0.05%	0.00%

[4] – University of Arizona. “Dimension and thermal properties of the chip.” D2L Course Content. Accessed March 22, 2026. https://d2l.arizona.edu/d2l/le/content/1721202/viewContent/20387635/View

[5] Python script used within ANSYS to export images of each chip layer:

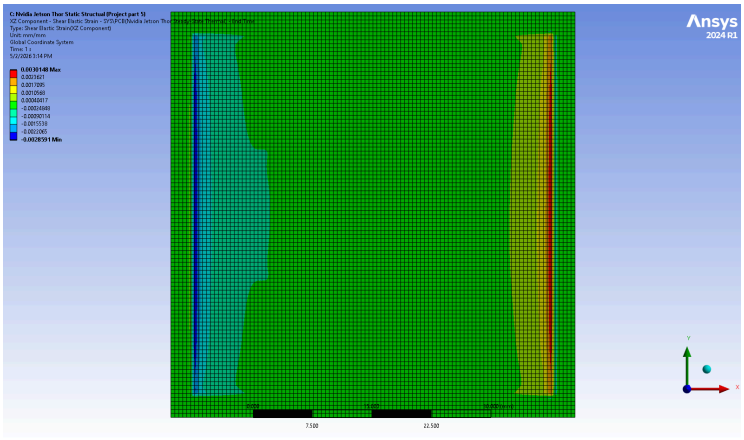
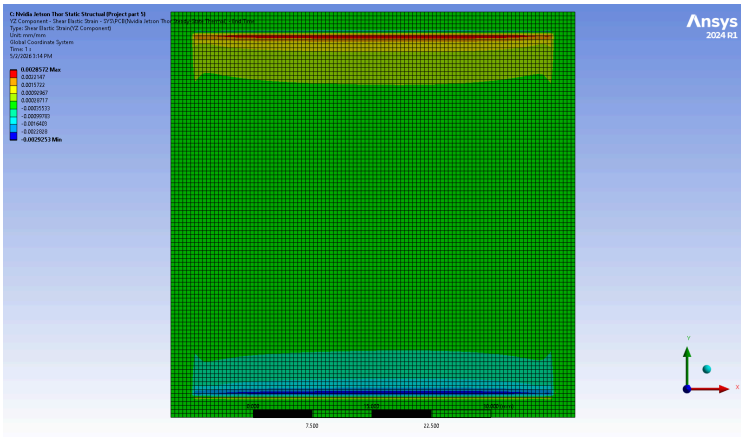
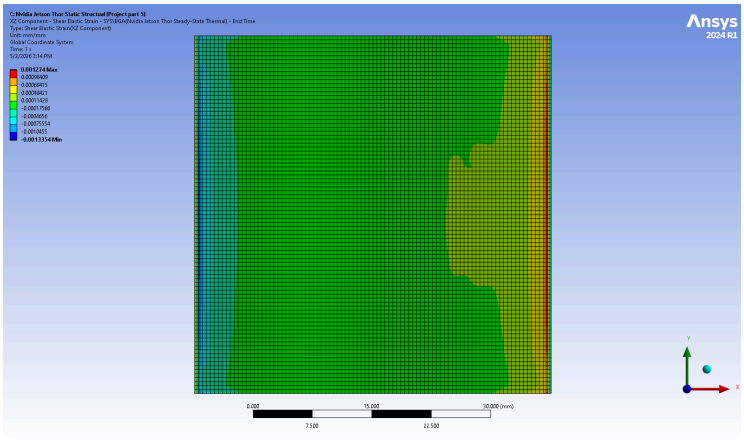
```
analysis = ExtAPI.DataModel.Project.Model.Analyses[0]
solution = analysis.Solution

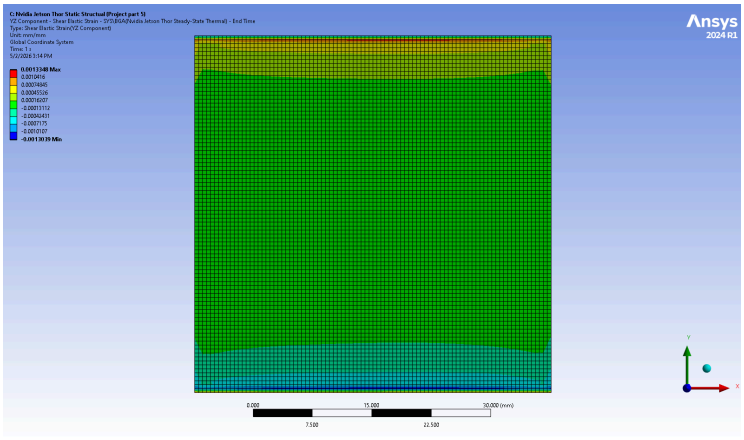
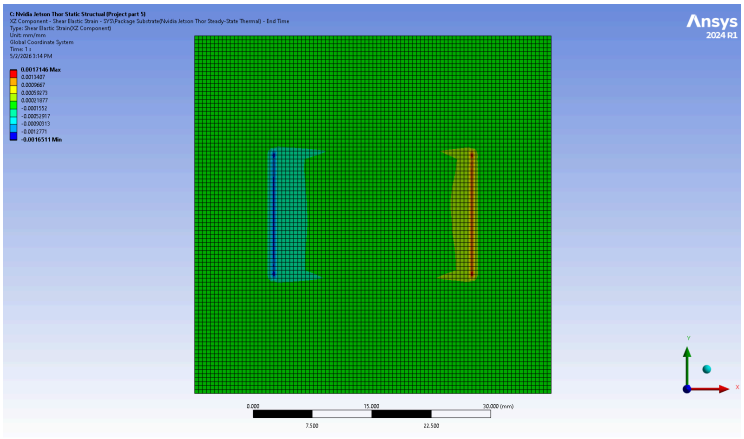
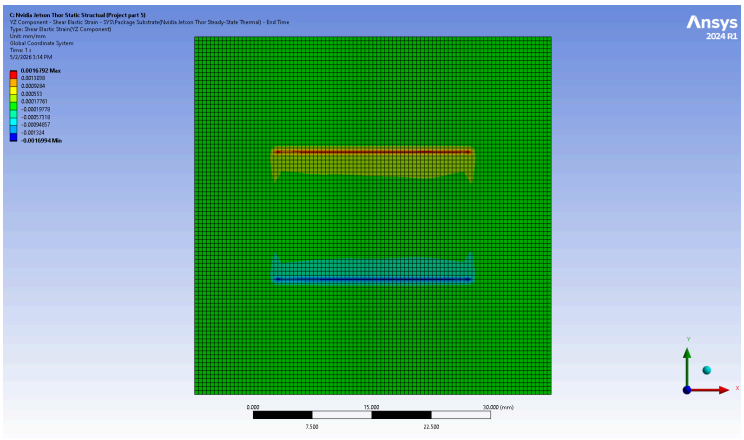
output_dir = r"C:\ANSYS\images"  # change this path

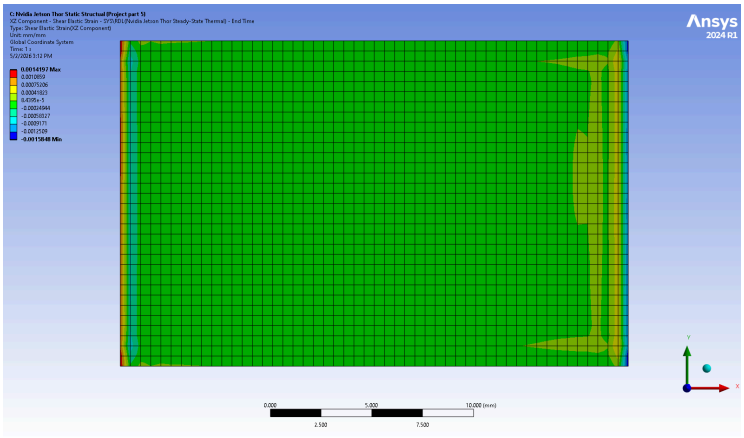
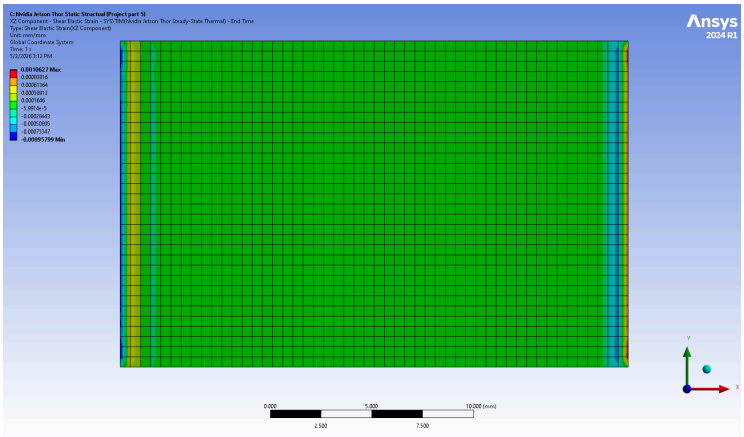
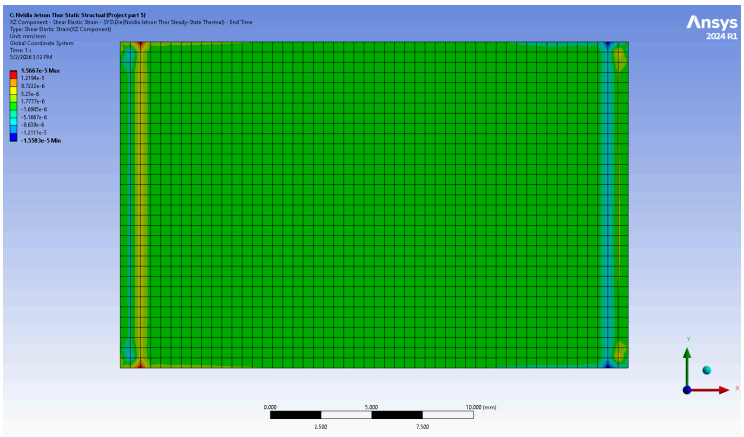
import os
if not os.path.exists(output_dir):
    os.makedirs(output_dir)

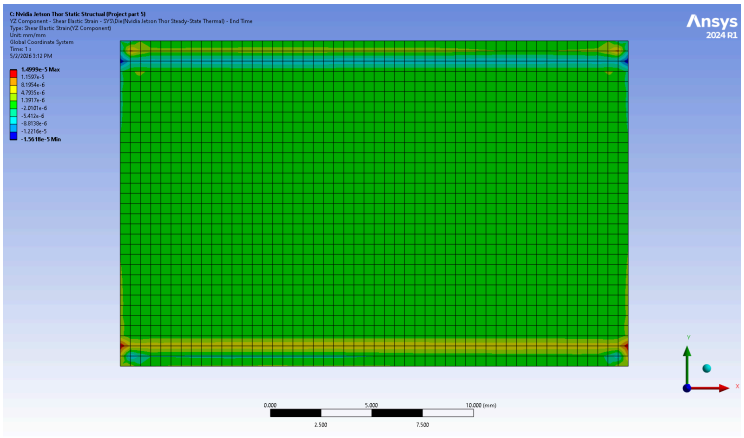
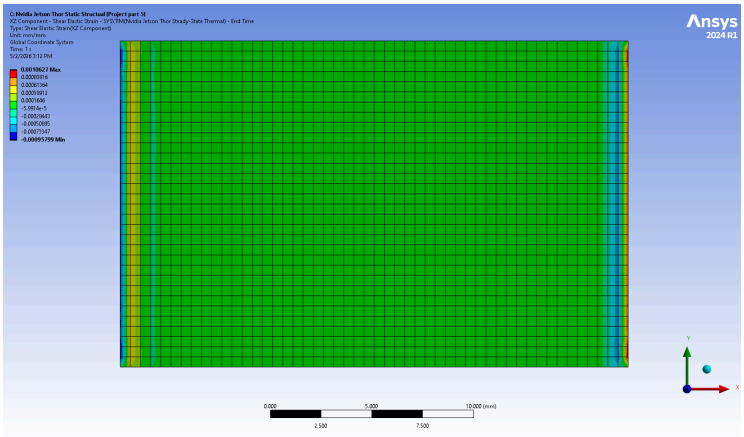
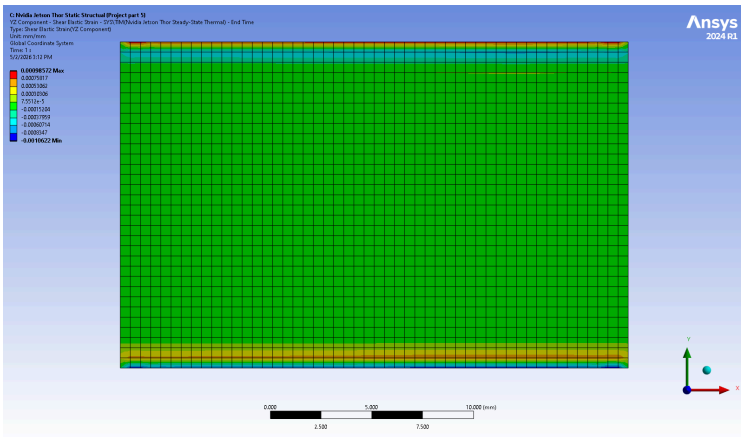
for result in solution.Children:
    try:
        result.Activate()
        filename = result.Name.replace(" ", "_") + ".png"
        fullpath = os.path.join(output_dir, filename)
        ExtAPI.Graphics.ExportImage(fullpath)
    except:
        Pass
```

[6] Table 3: Strain results across every device layer for powermap 1:

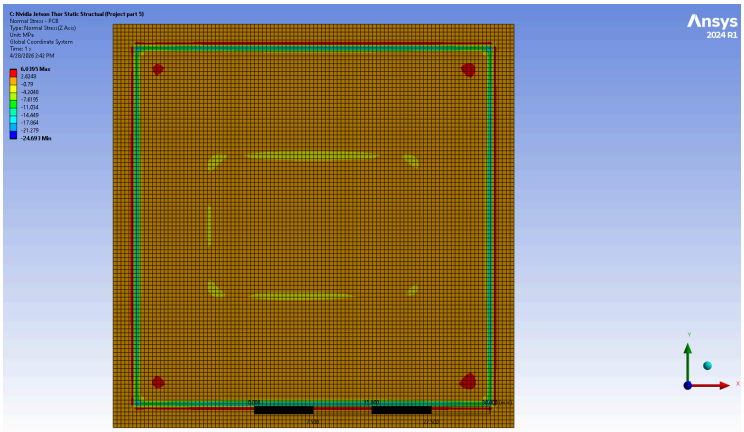
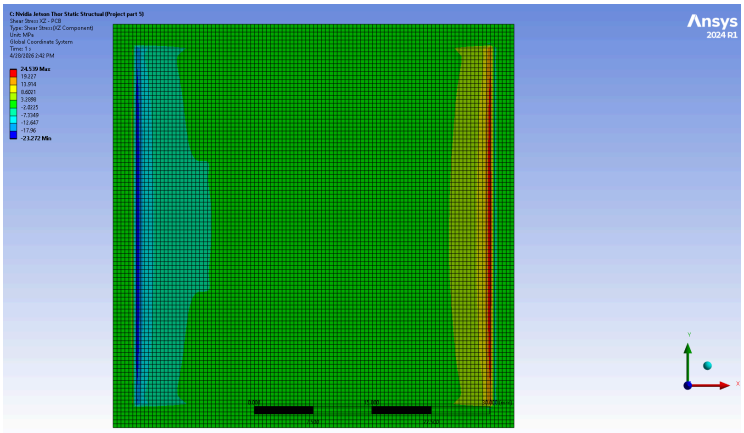
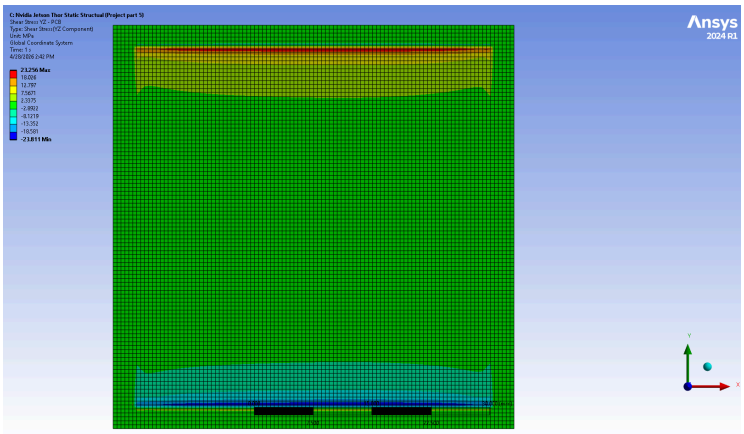
Layer	Strain type	Image
PCB	Strain γ_xz	
	Strain γ_yz	
BGA	Strain γ_xz	

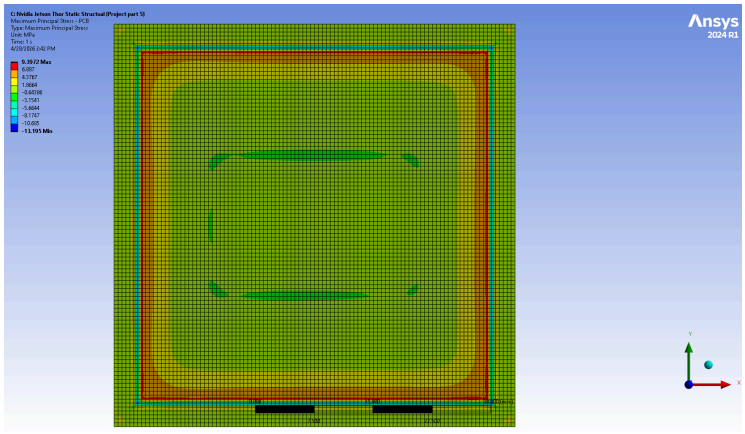
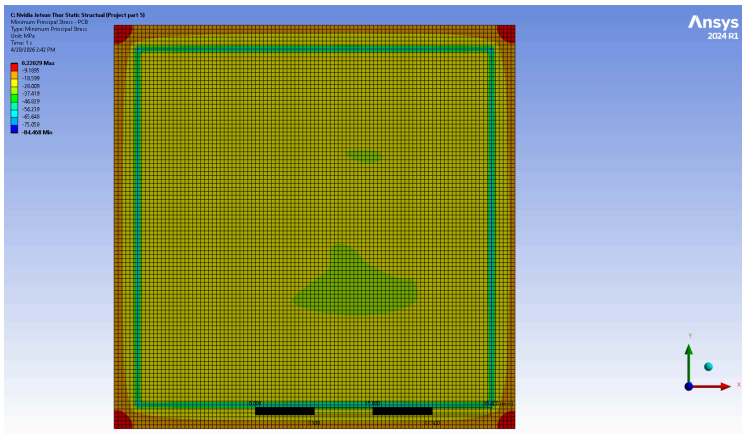
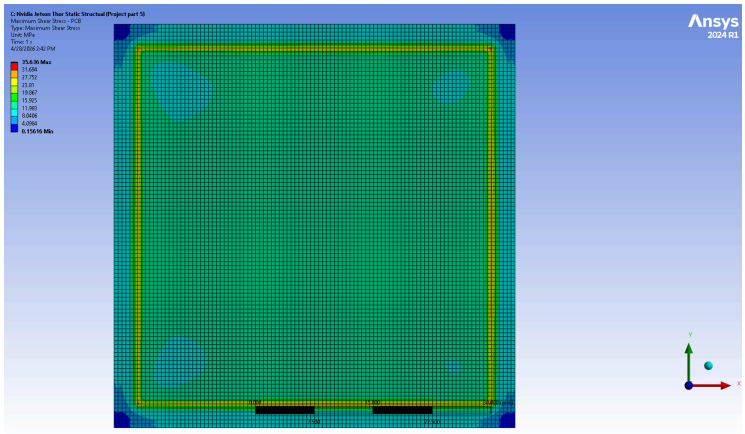
	Strain γ_yz	
Package Substrate	Strain γ_xz	
	Strain γ_yz	

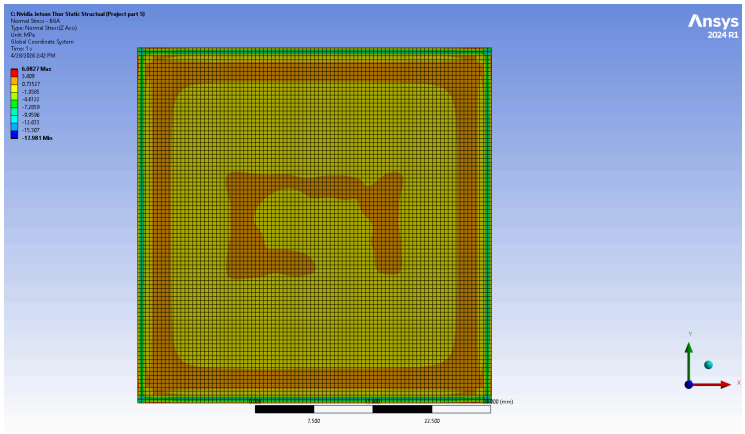
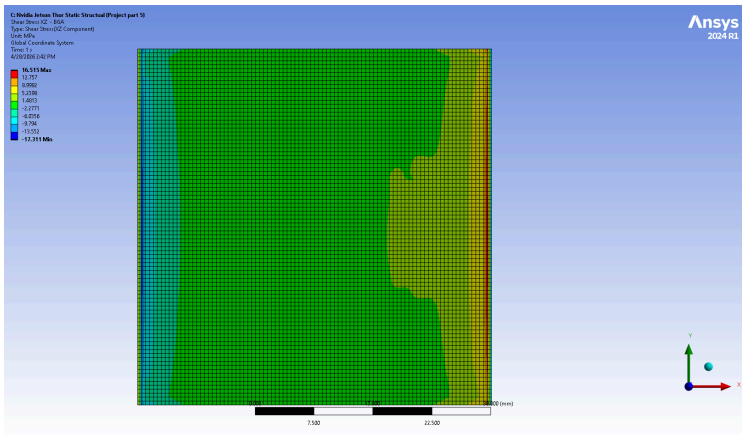
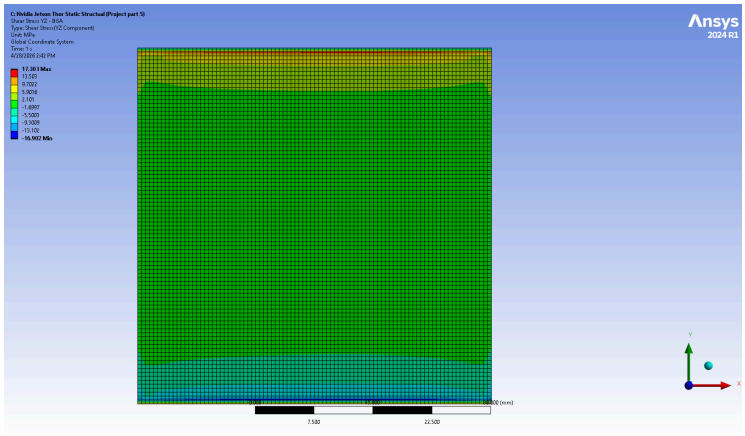
RDL	Strain γ_xz	
	Strain γ_yz	
Die	Strain γ_xz	

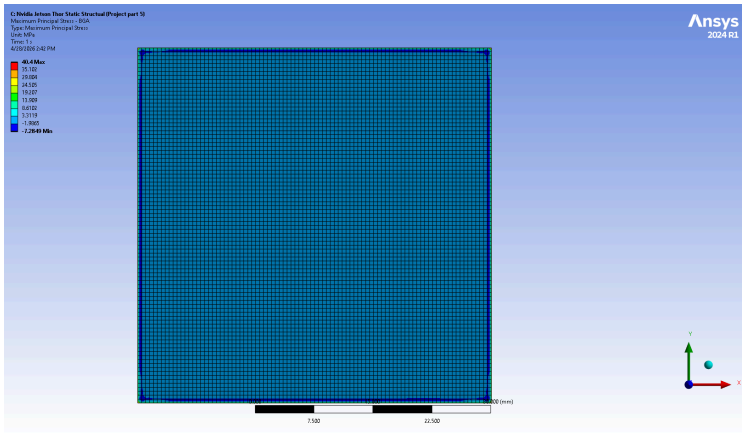
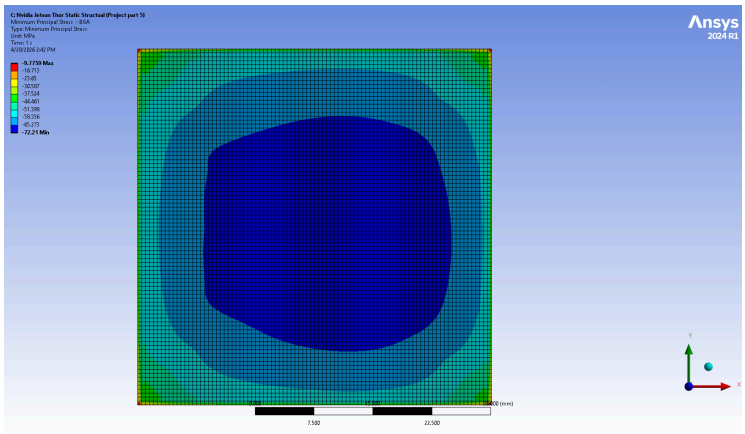
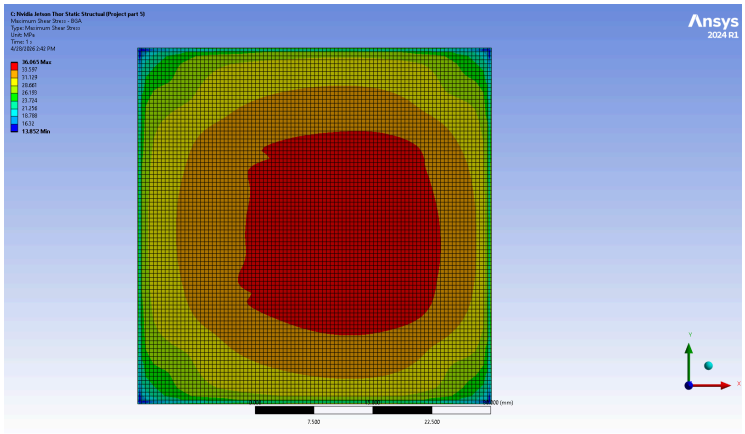
	Strain γ_yz	
TIM	Strain γ_xz	
	Strain γ_yz	

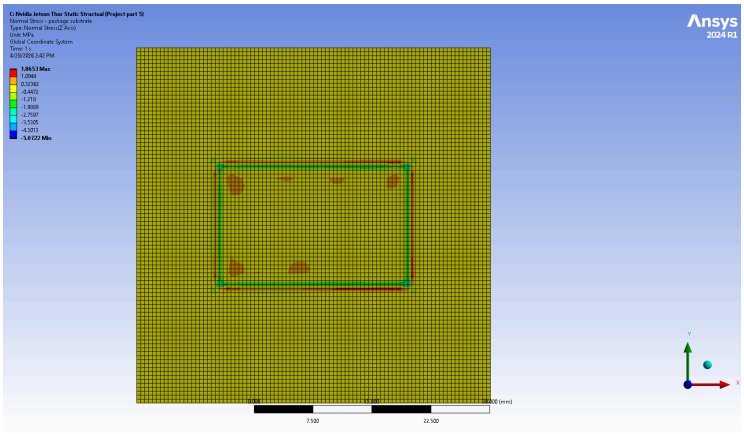
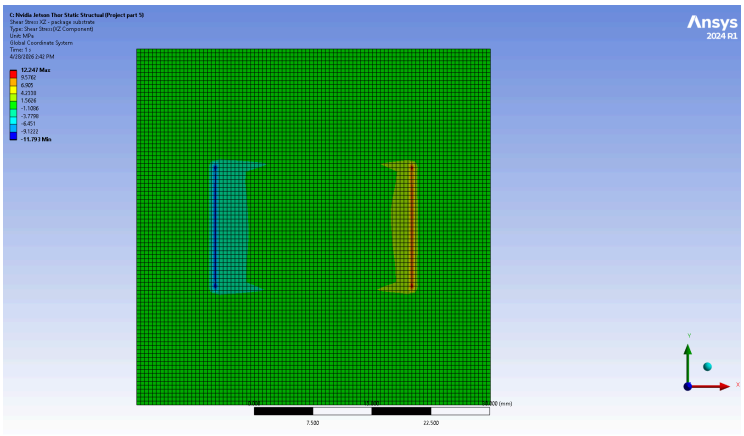
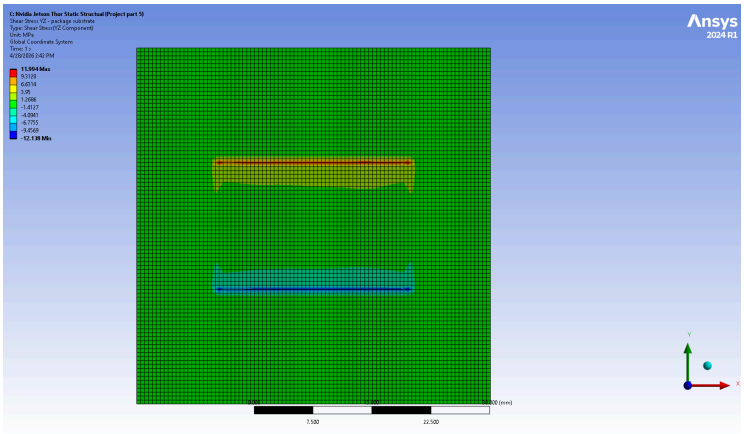
[7] Table 4: Stress results across every device layer for powermap 1:

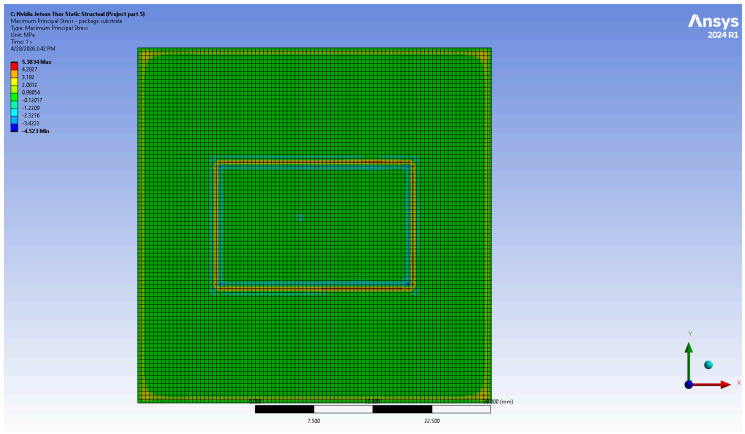
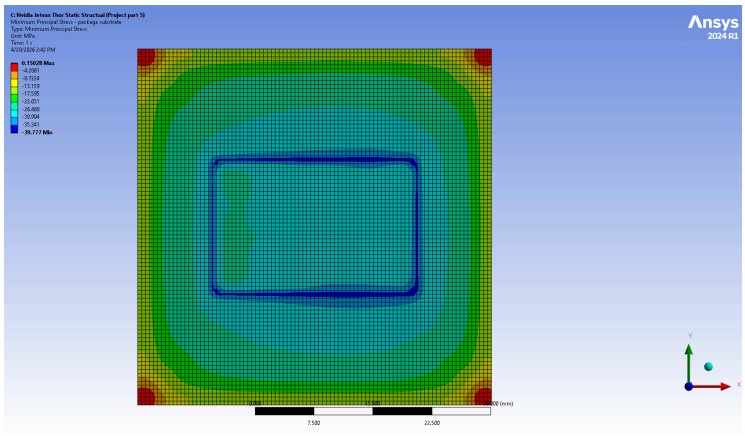
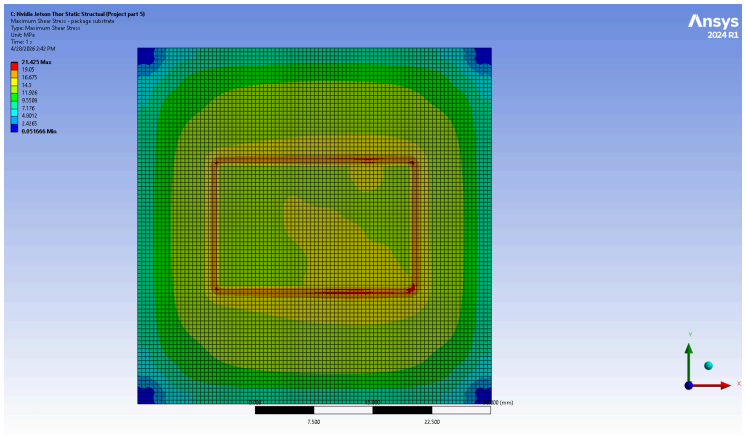
Layer	Stress type	Image
PCB	Normal σ_zz	
	Shear τ_xz	
	Shear τ_yz	

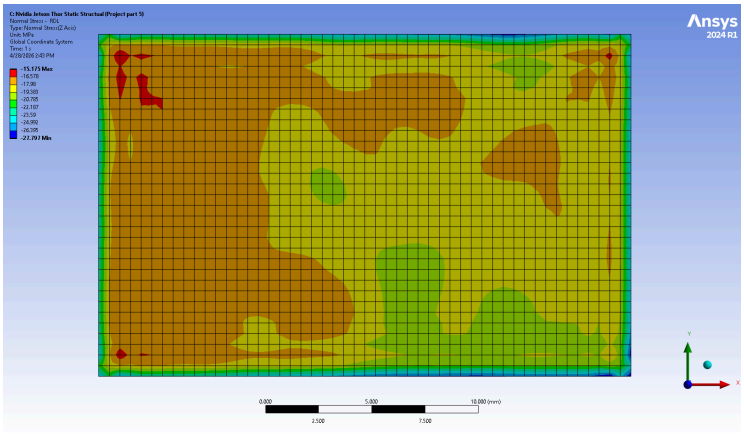
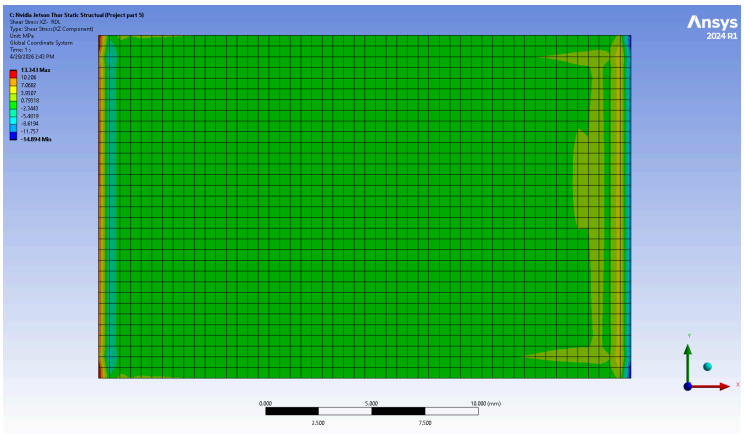
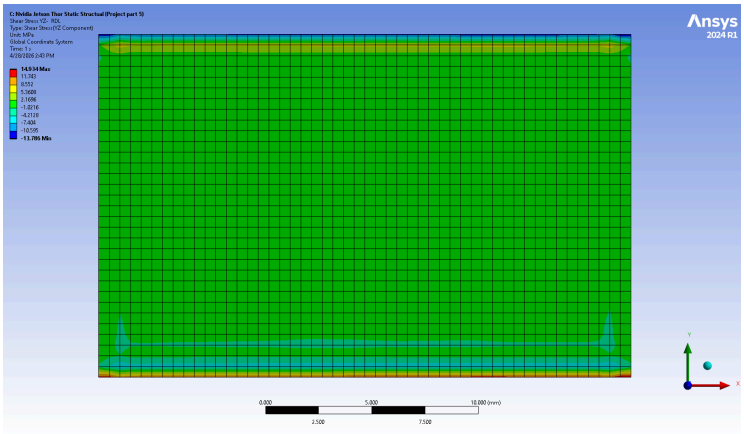
	Maximum Principal σ_1	
	Minimum Principal σ_3	
	Maximum Shear τ	

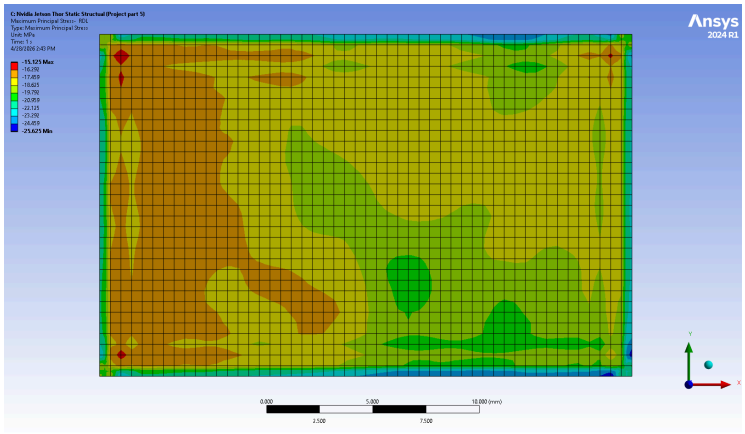
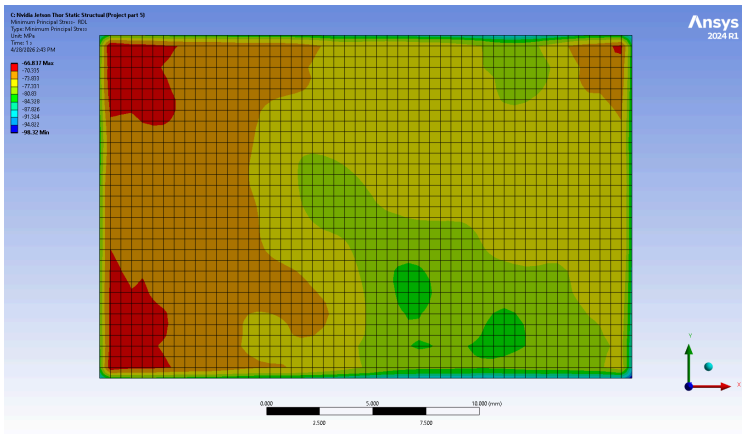
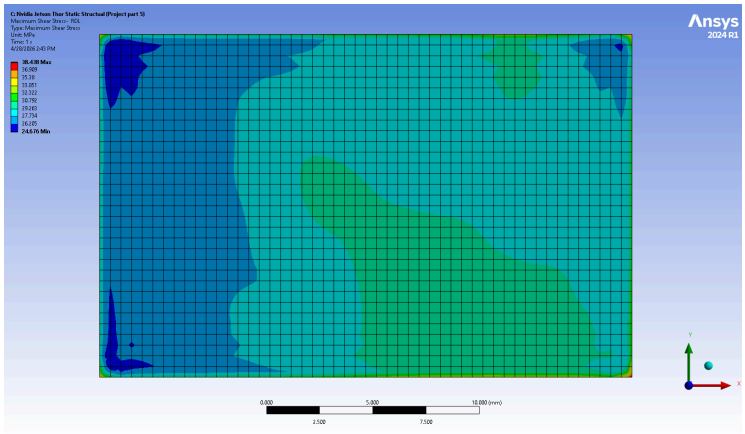
BGA	Normal σ_zz	
	Shear τ_xz	
	Shear τ_yz	

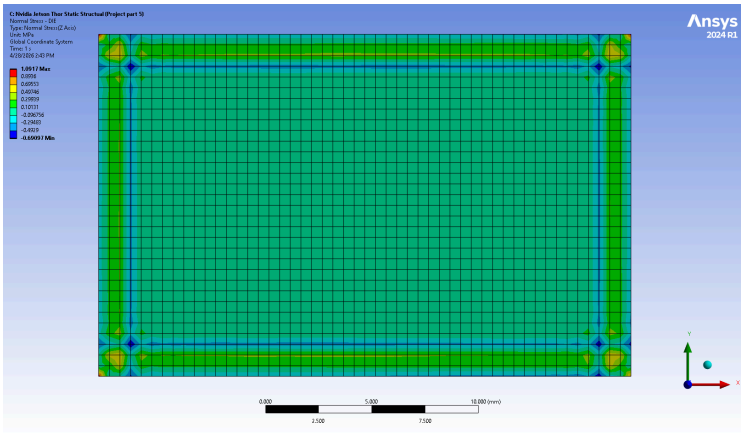
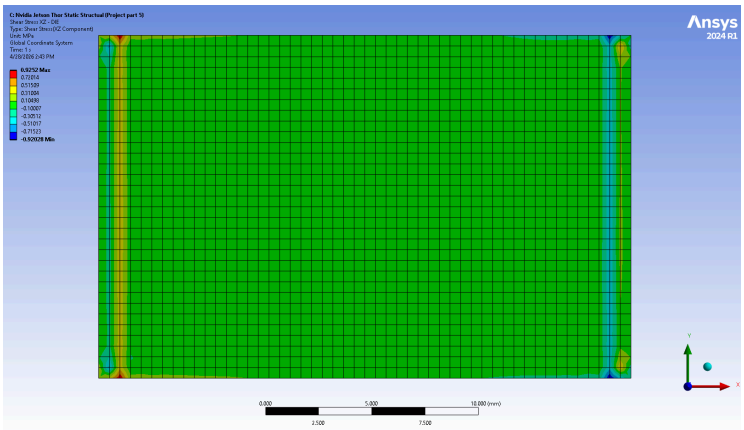
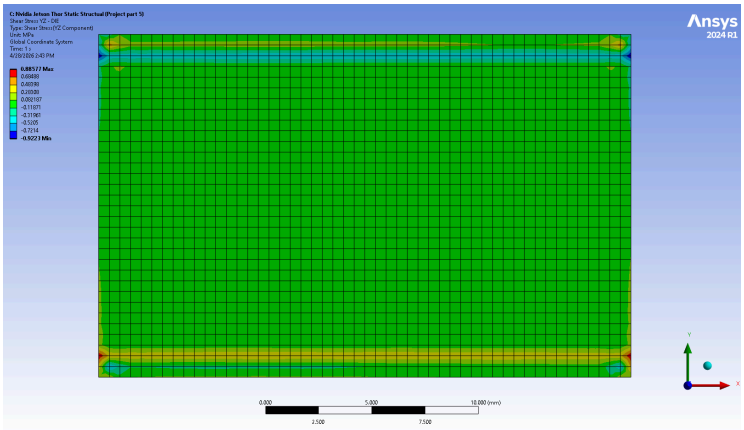
	Maximum Principal σ_1	
	Minimum Principal σ_3	
	Maximum Shear τ	

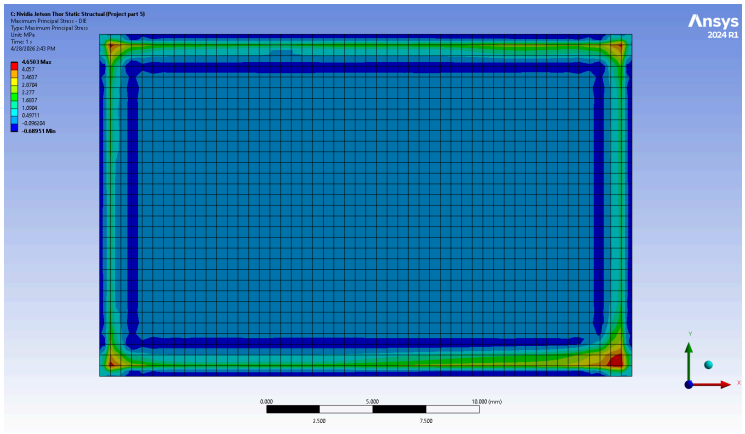
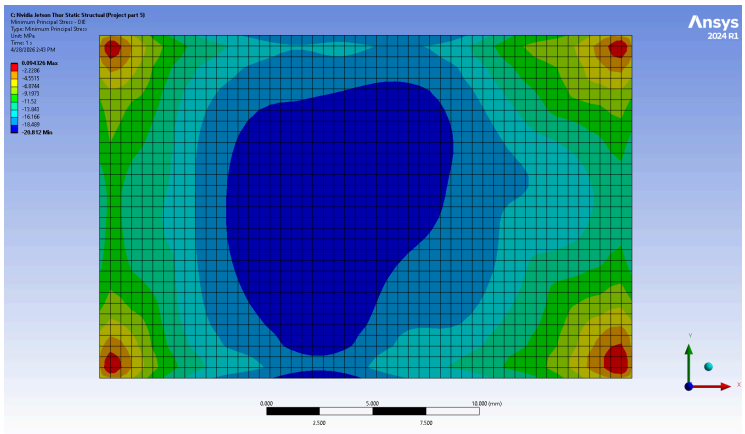
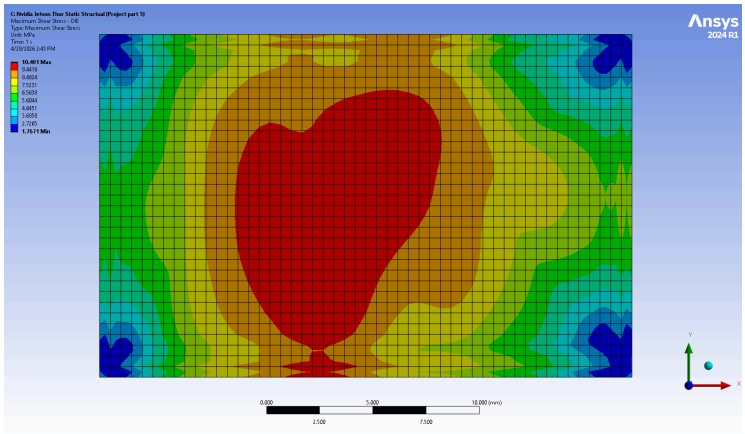
Package Substrate	Normal σ_zz	
	Shear τ_xz	
	Shear τ_yz	

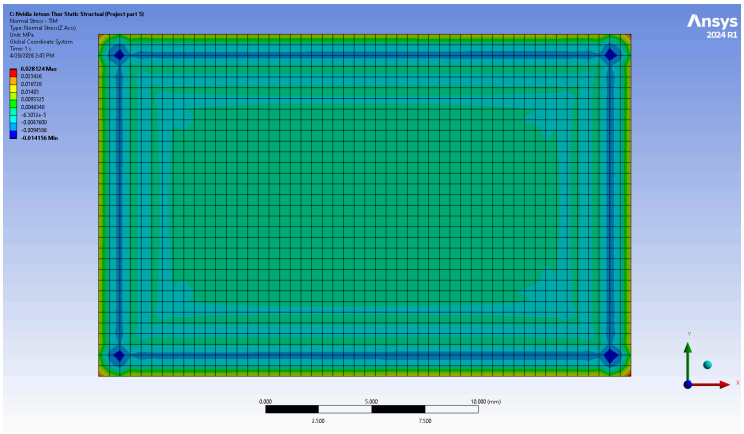
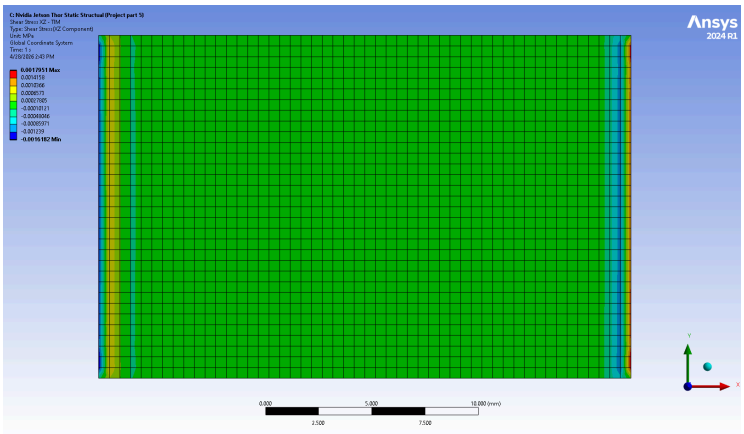
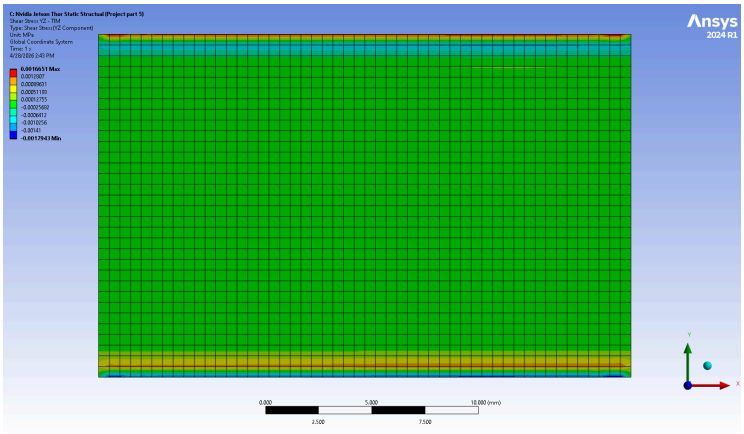
	Maximum Principal σ_1	
	Minimum Principal σ_3	
	Maximum Shear τ	

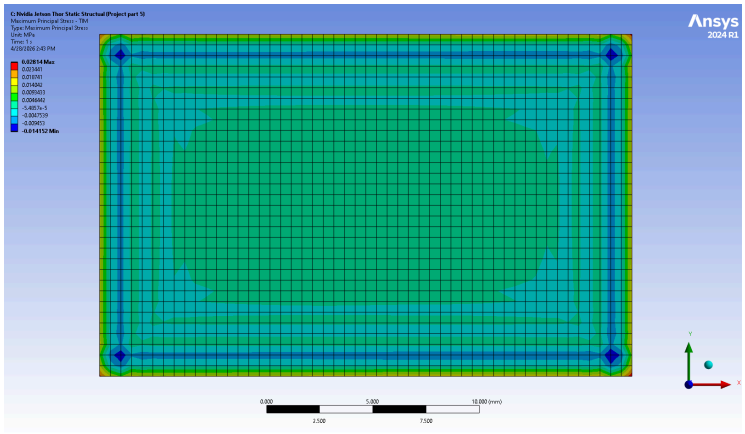
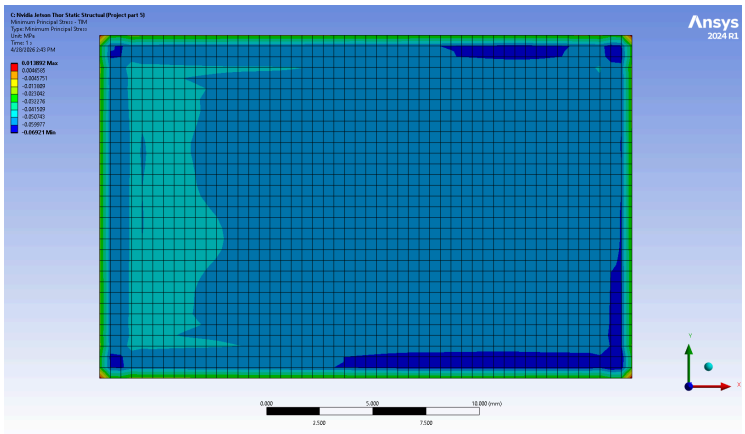
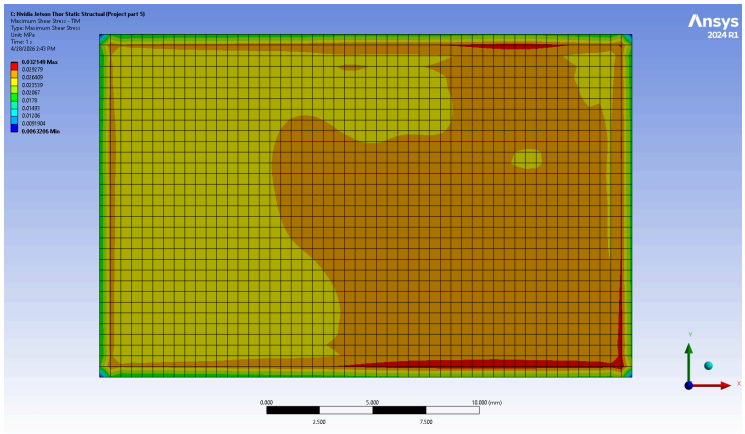
RDL	Normal σ_zz	
	Shear τ_xz	
	Shear τ_yz	

	Maximum Principal σ_1	
	Minimum Principal σ_3	
	Maximum Shear τ	

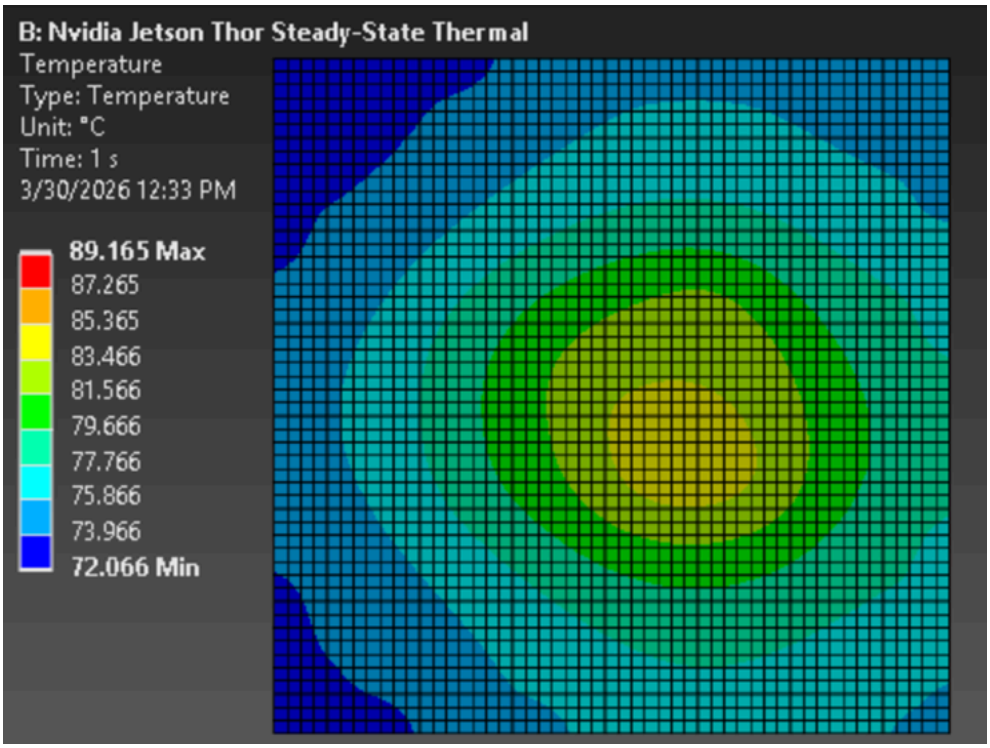
DIE	Normal σ_zz	
	Shear τ_xz	
	Shear τ_yz	

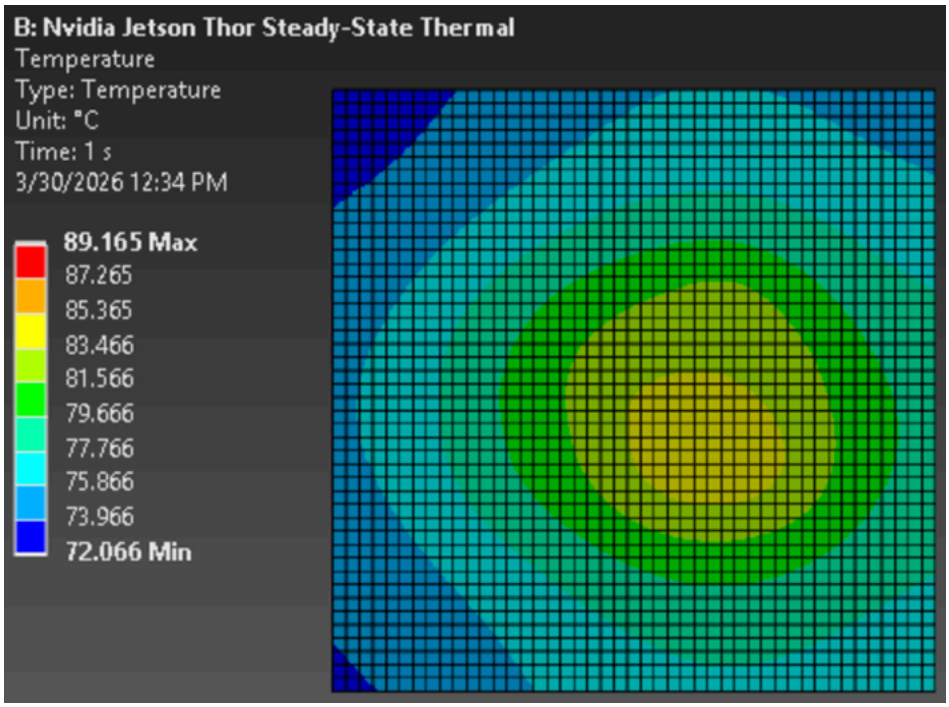
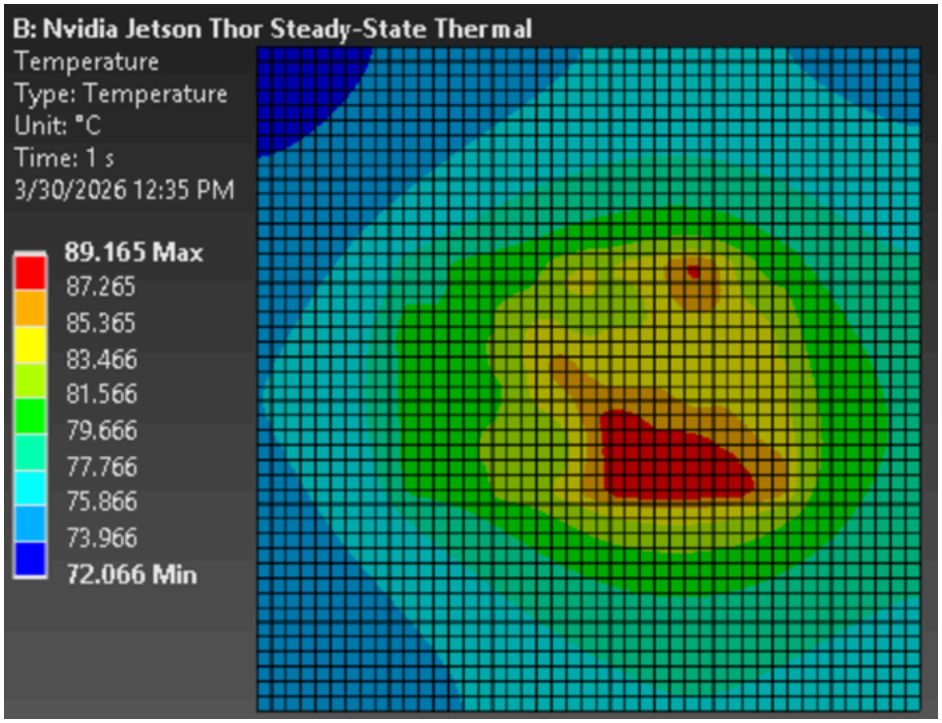
	Maximum Principal σ_1	
	Minimum Principal σ_3	
	Maximum Shear τ	

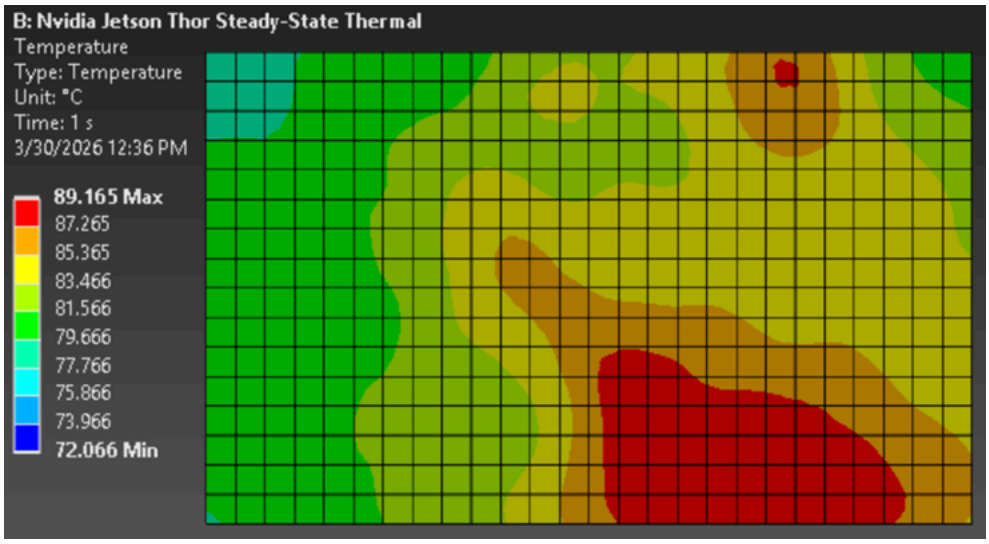
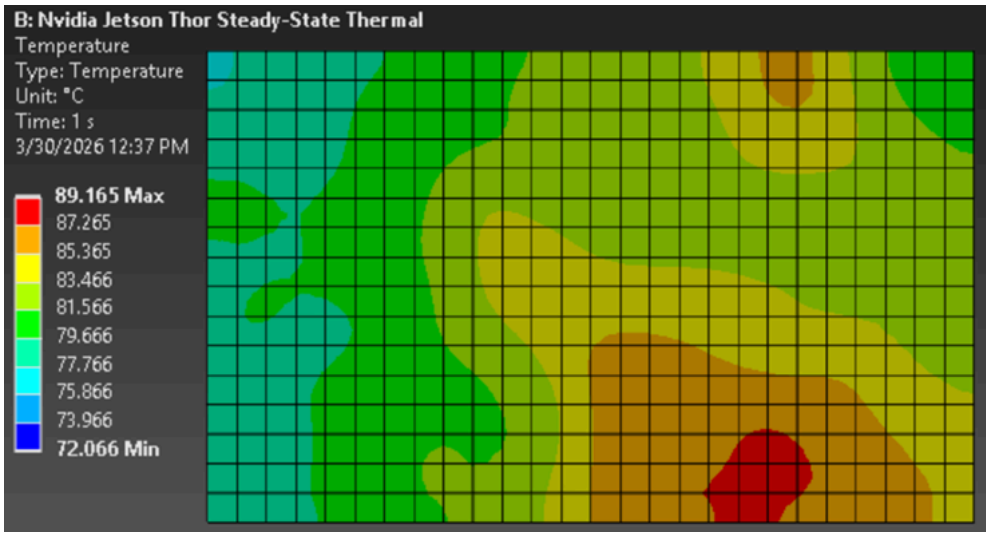
TIM	Normal σ_zz	
	Shear τ_xz	
	Shear τ_yz	

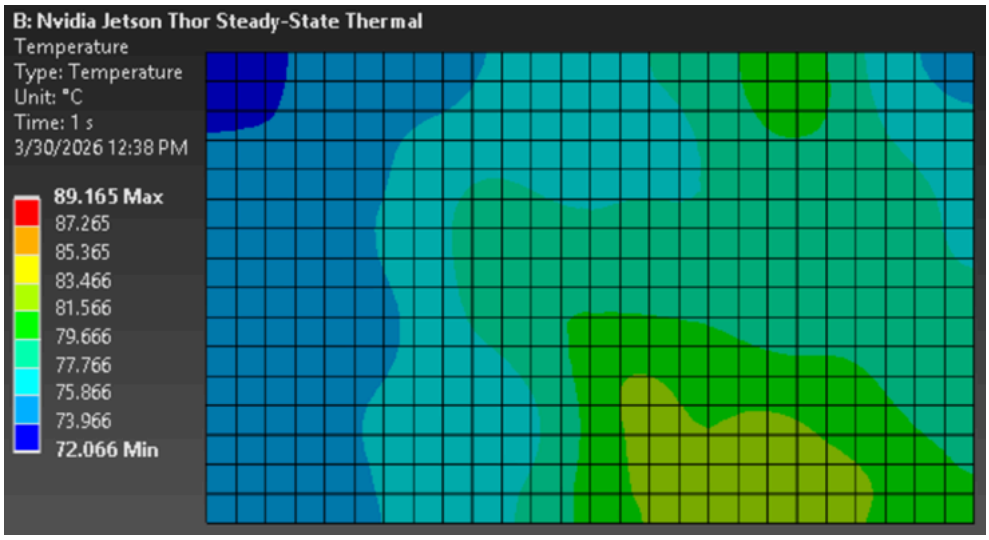
	Maximum Principal σ_1	
	Minimum Principal σ_3	
	Maximum Shear τ	

[8] – Table 5: Temperature distribution across each device layer of the Nvidia Thor Jetson chip corresponding to powermap 1:

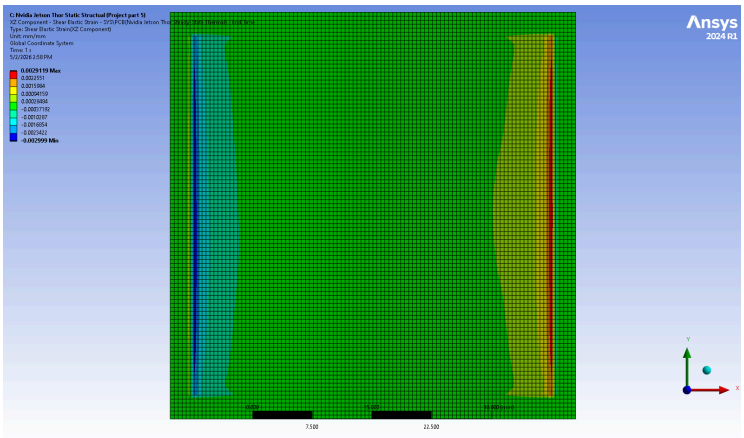
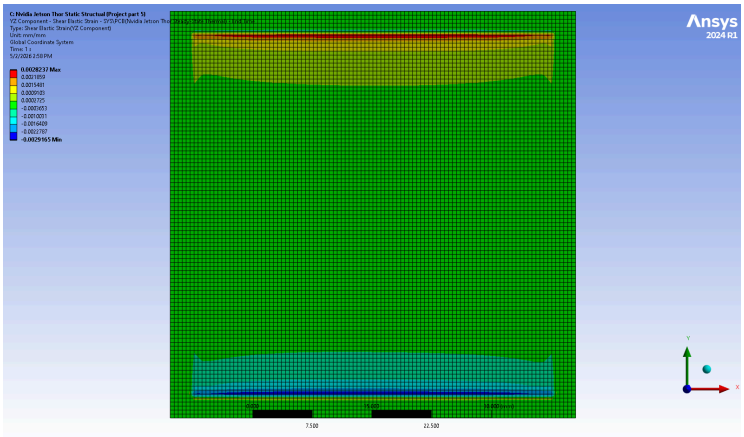
Device Layer	**Temperature Distribution**
PCB	

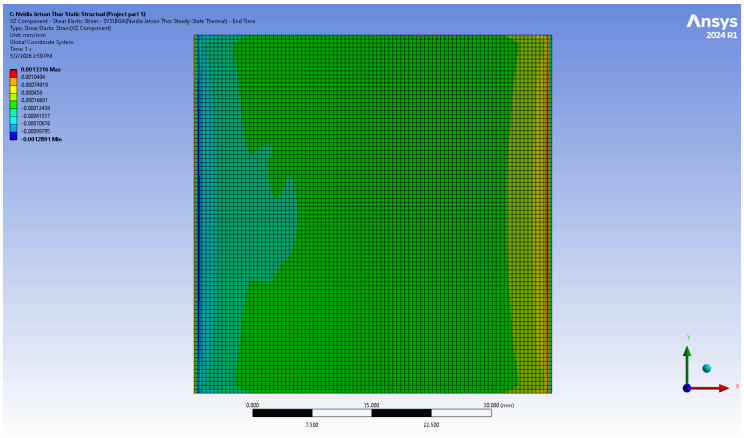
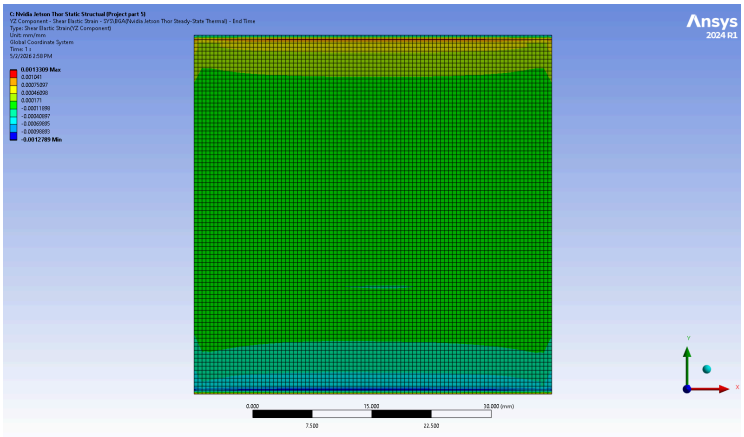
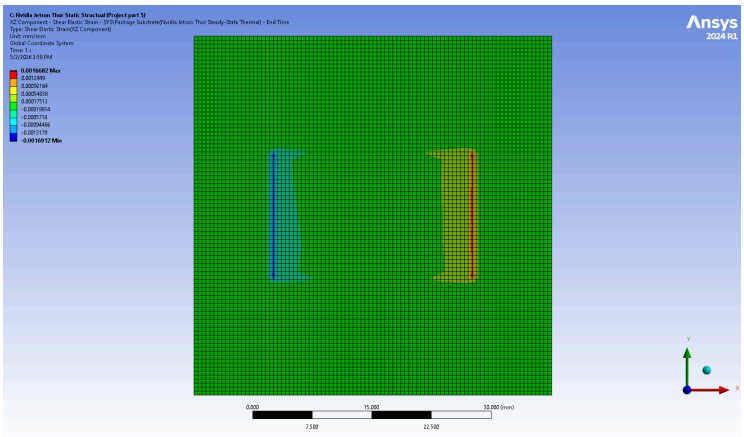
BGA	
Package Substrate	

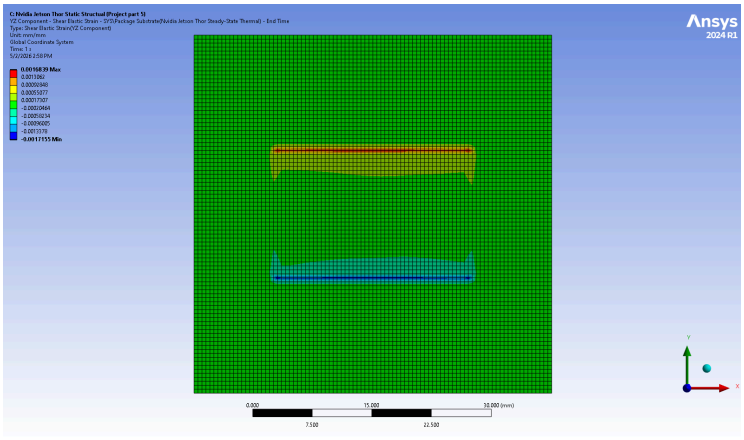
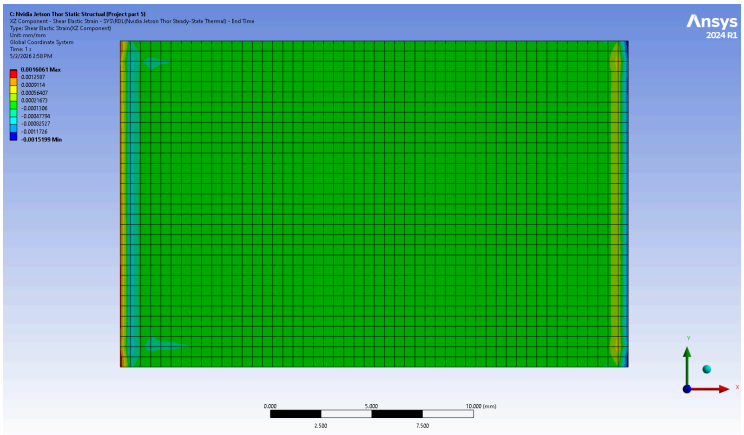
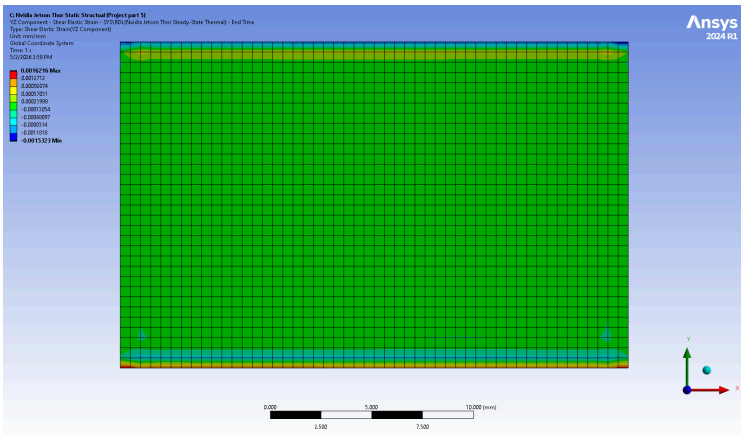
RDL	B: Nvidia Jetson Thor Steady-State Thermal Temperature Type: Temperature Unit: °C Time: 1 s 3/30/2026 12:36 PM 89.165 Max 87.265 85.365 83.466 81.566 79.666 77.766 75.866 73.966 72.066 Min
DIE	B: Nvidia Jetson Thor Steady-State Thermal Temperature Type: Temperature Unit: °C Time: 1 s 3/30/2026 12:37 PM 89.165 Max 87.265 85.365 83.466 81.566 79.666 77.766 75.866 73.966 72.066 Min

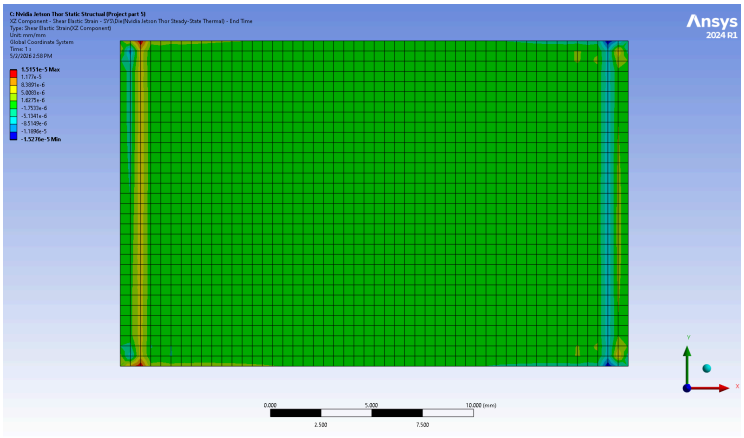
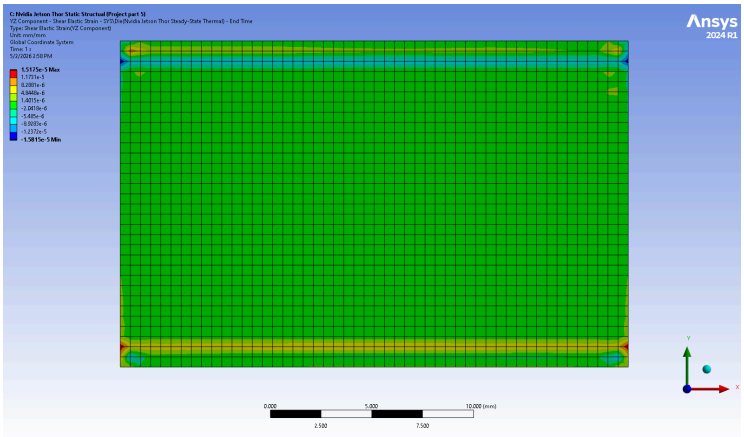
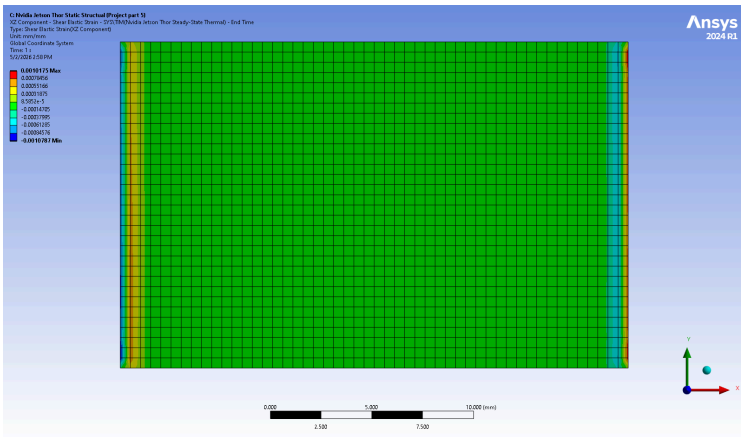
TIM	

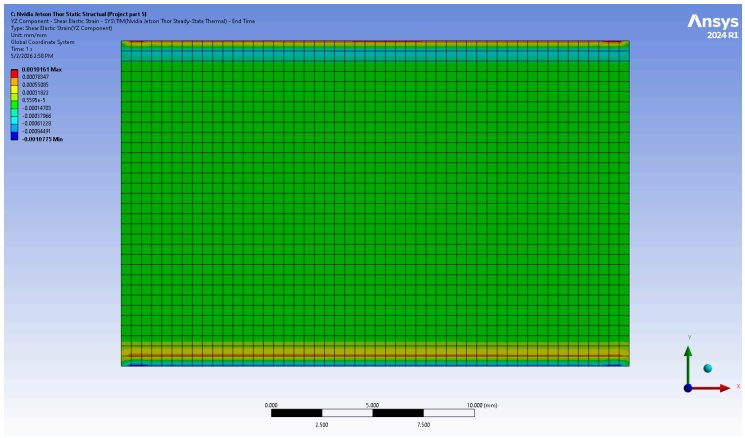
[9] Table 6: Strain results across every device layer for powermap 2:

Layer	**Strain type**	**Image**
PCB	Strain τ_xz	
	Strain γ_yz	

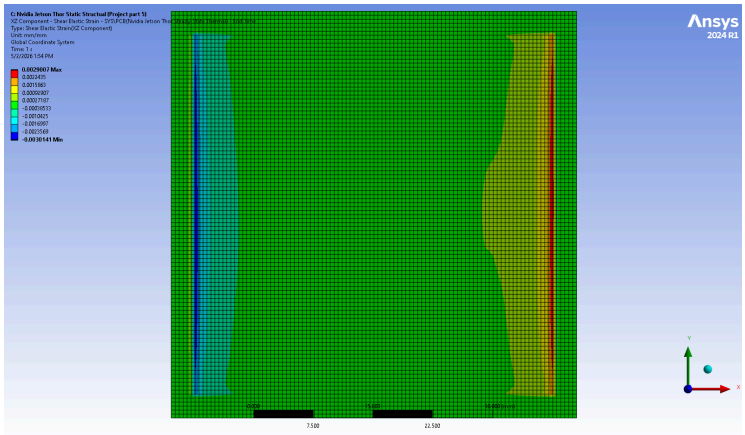
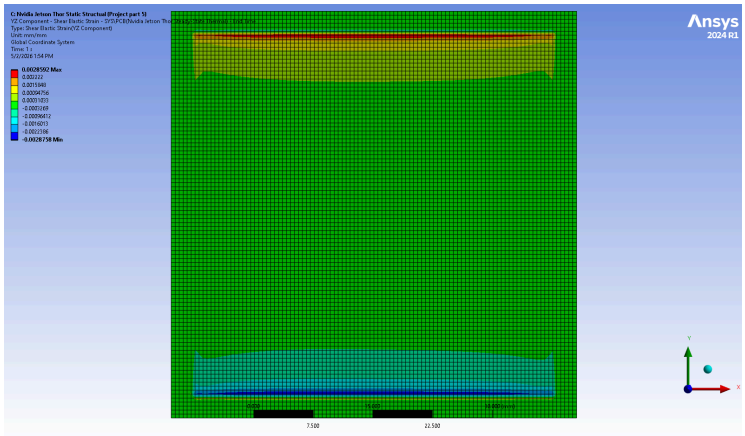
BGA	Strain γ_xz	
	Strain γ_yz	
Package Substrate	Strain γ_xz	

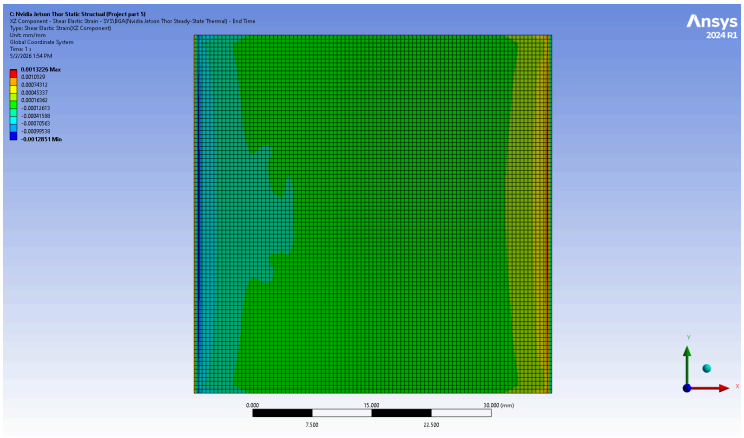
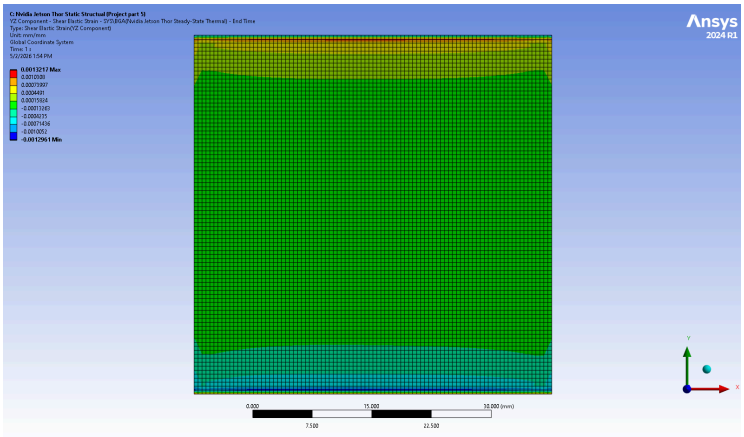
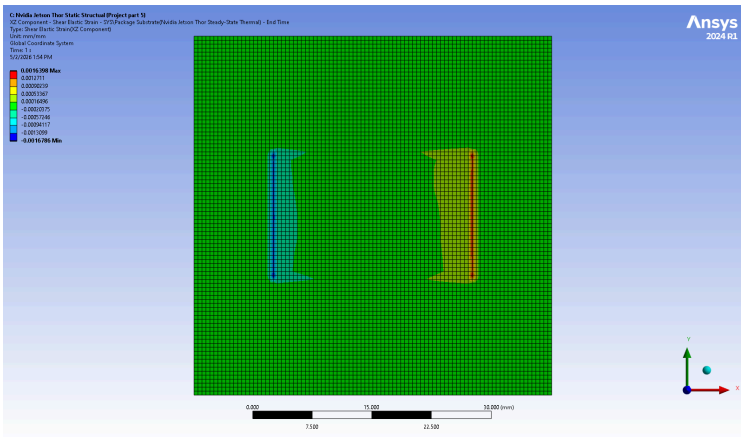
	Strain γ_yz	
RDL	Strain γ_xz	
	Strain γ_yz	

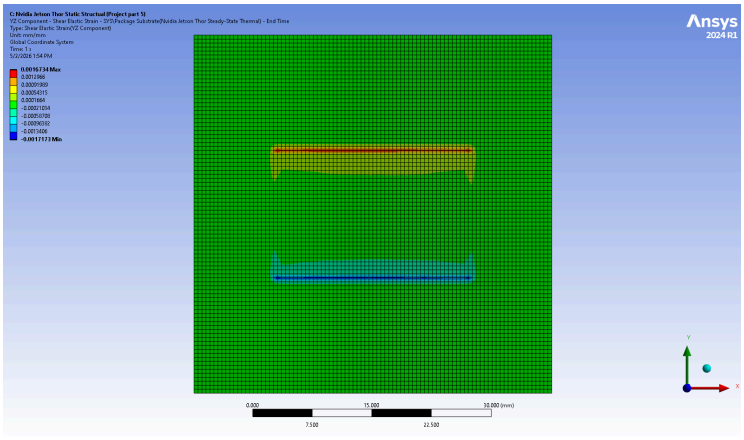
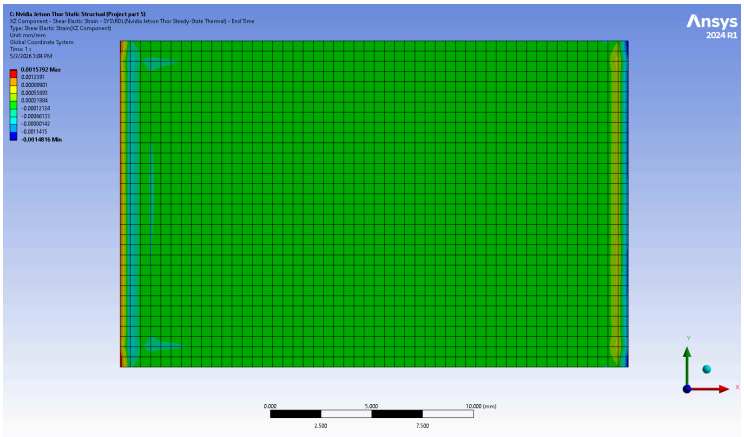
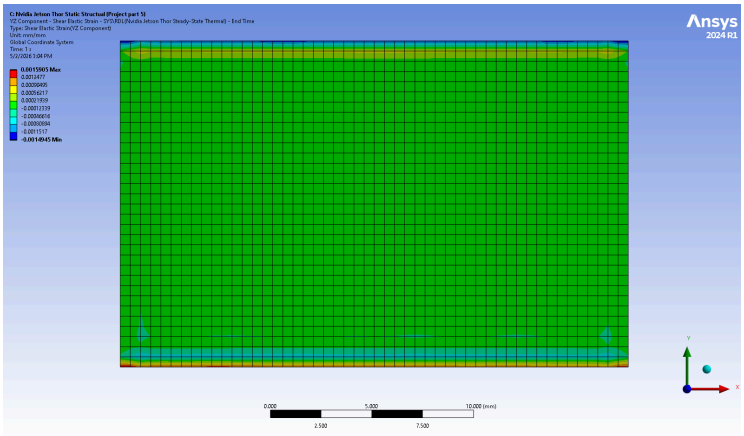
Die	Strain γ_xz	
	Strain γ_yz	
TIM	Strain γ_xz	

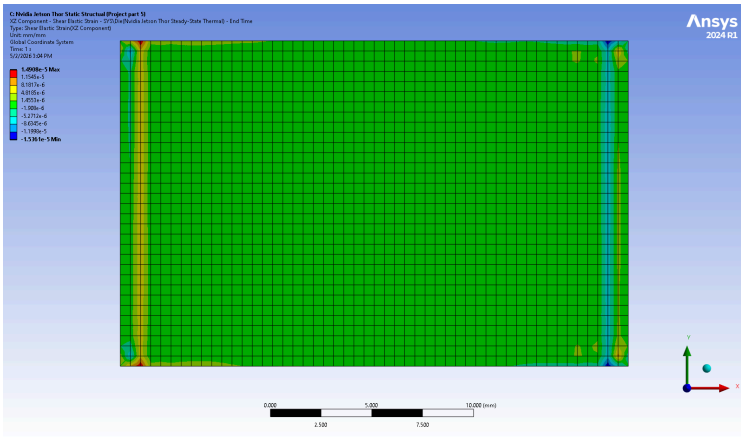
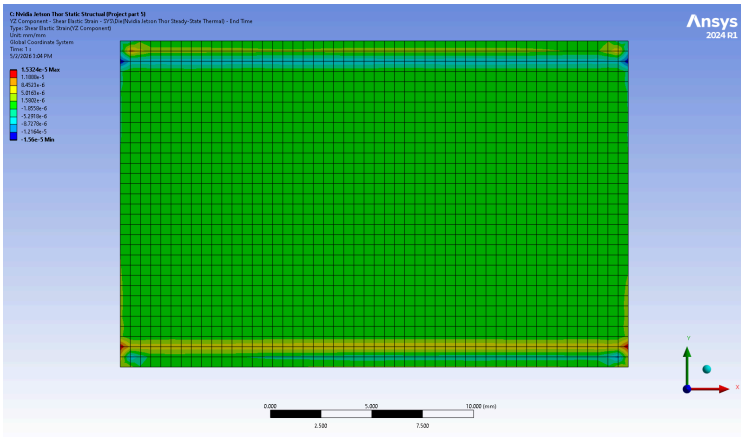
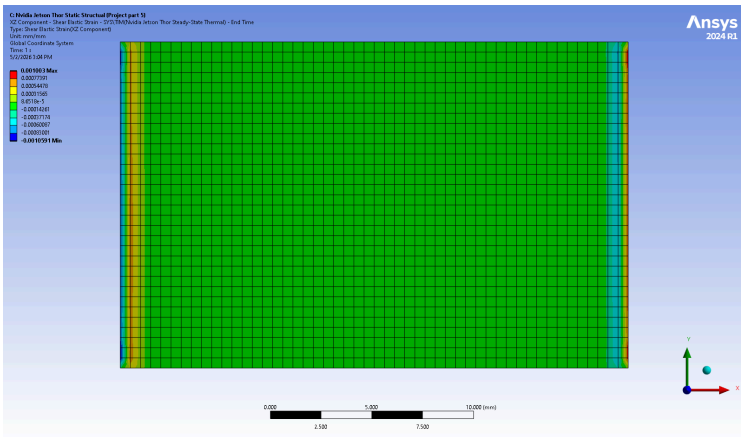
	Strain γ_yz	

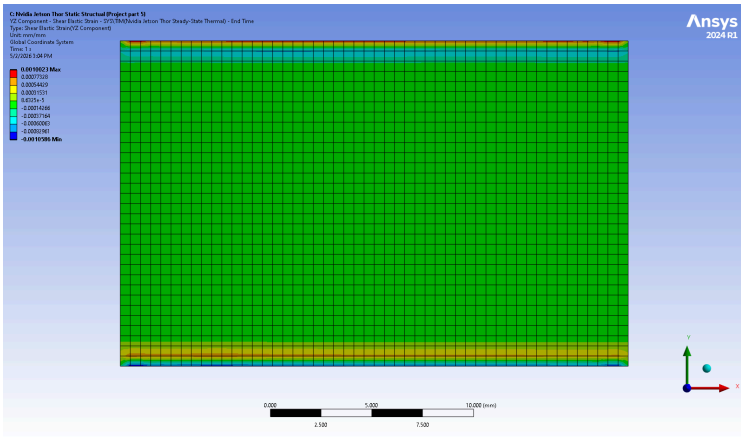
[10] Table 7: Strain results across every device layer for powermap 3:

Layer	**Strain type**	**Image**
PCB	Strain γ_xz	
	Strain γ_yz	

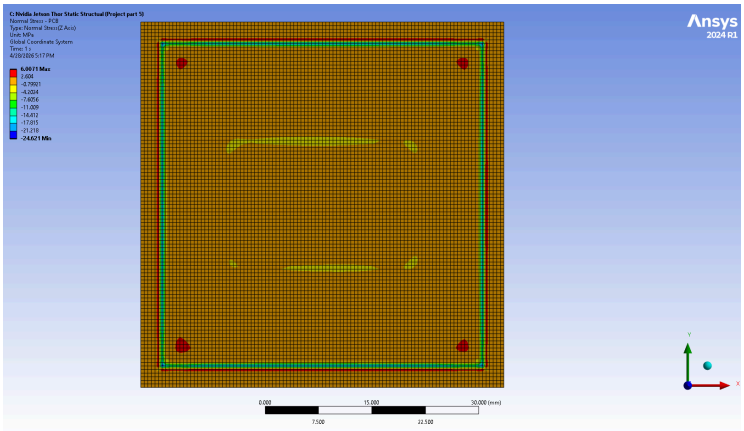
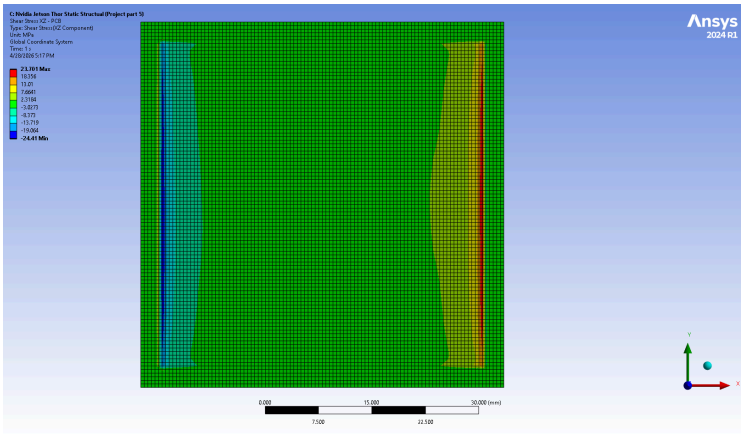
BGA	Strain γ_xz	
	Strain γ_yz	
Package Substrate	Strain γ_xz	

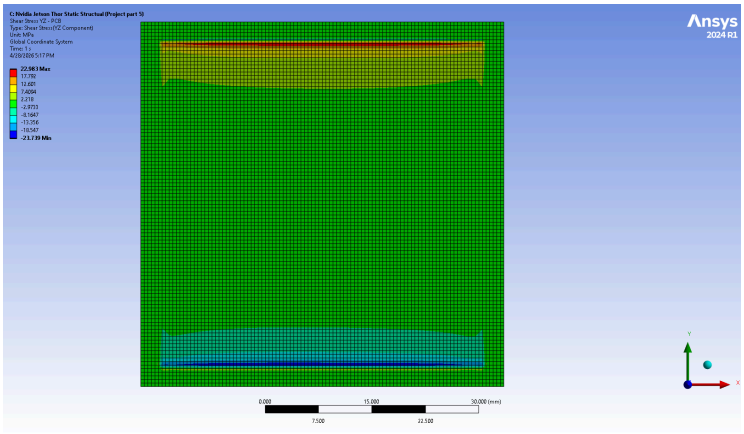
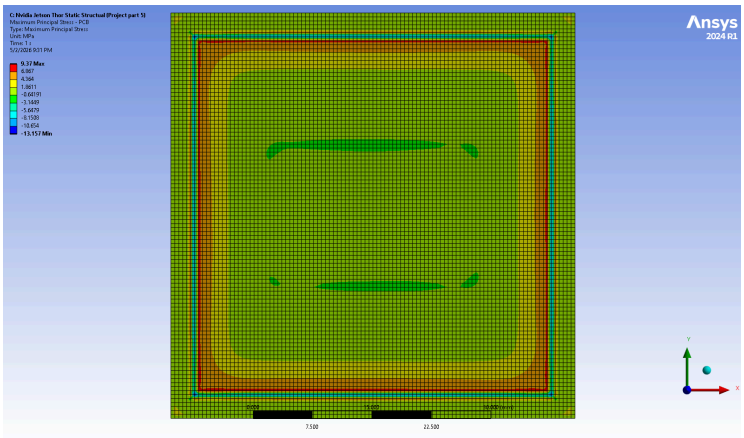
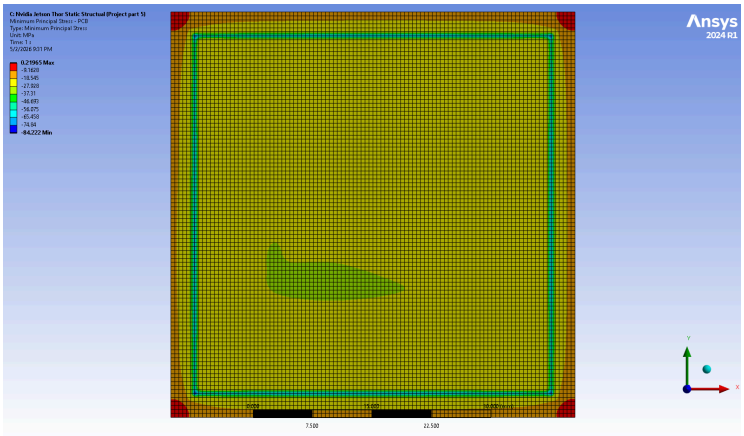
	Strain γ_yz	
RDL	Strain γ_xz	
	Strain γ_yz	

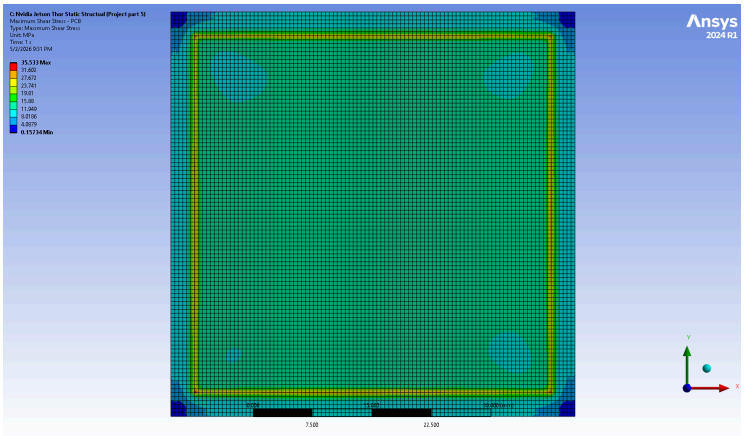
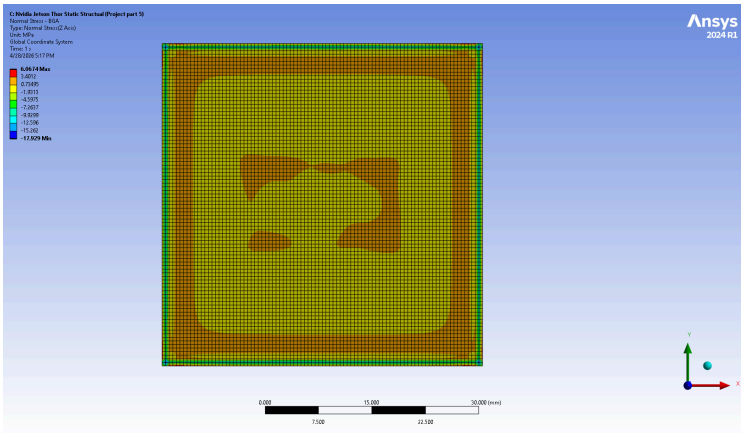
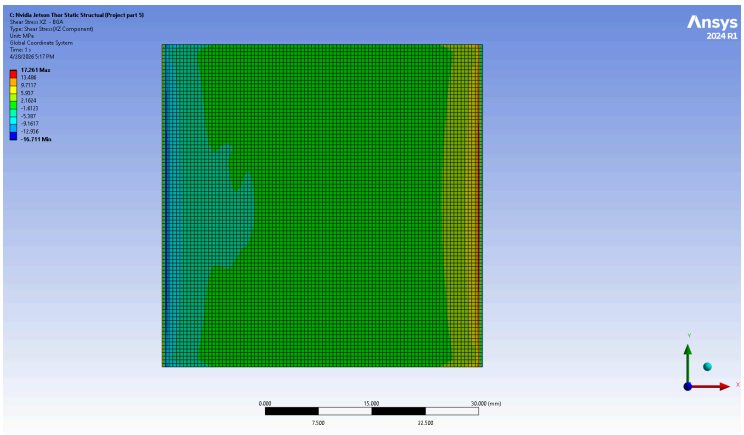
Die	Strain γ_xz	
	Strain γ_yz	
TIM	Strain γ_xz	

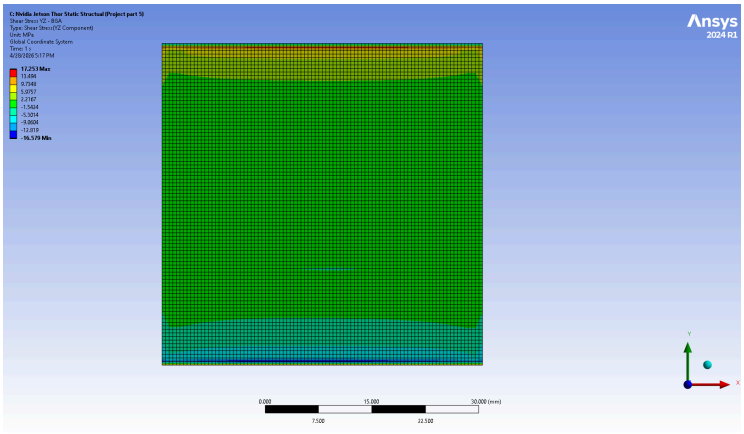
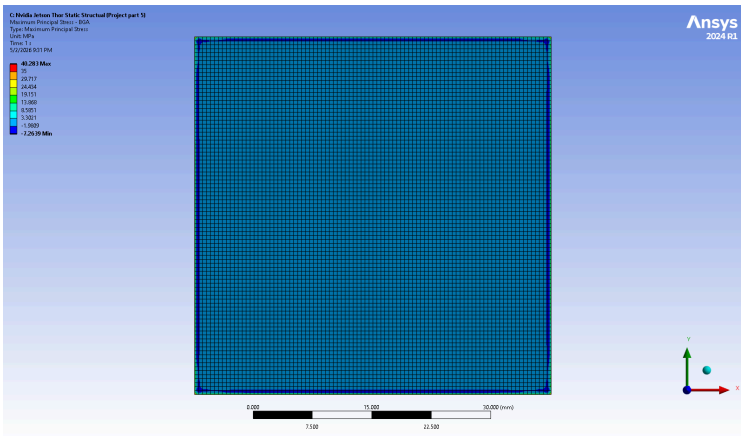
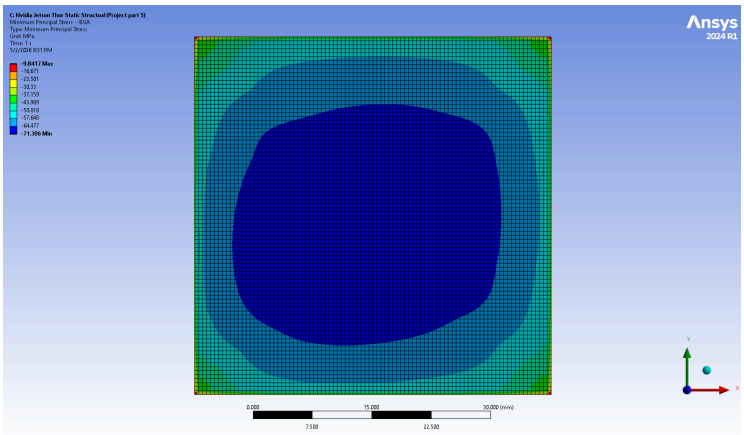
	Strain γ_yz	

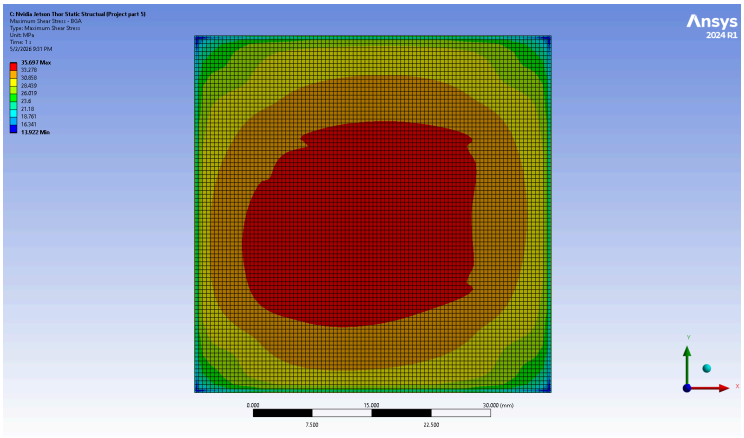
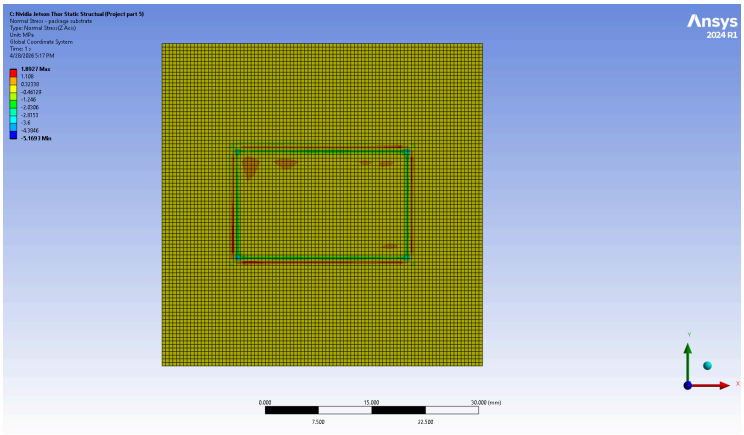
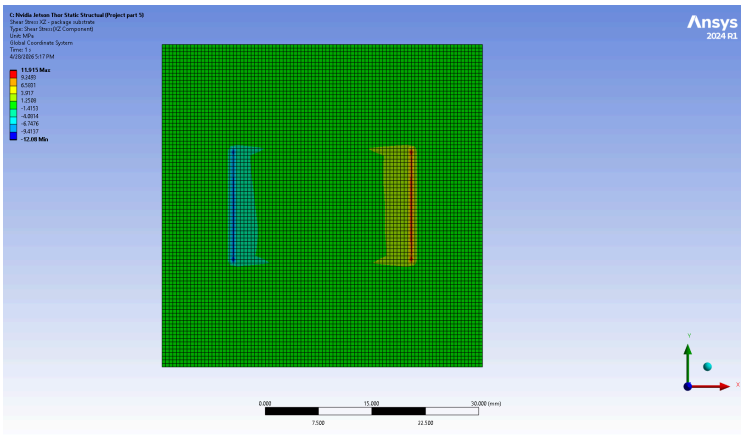
[11] Table 8: Stress results for across every device layer for powermap 2:

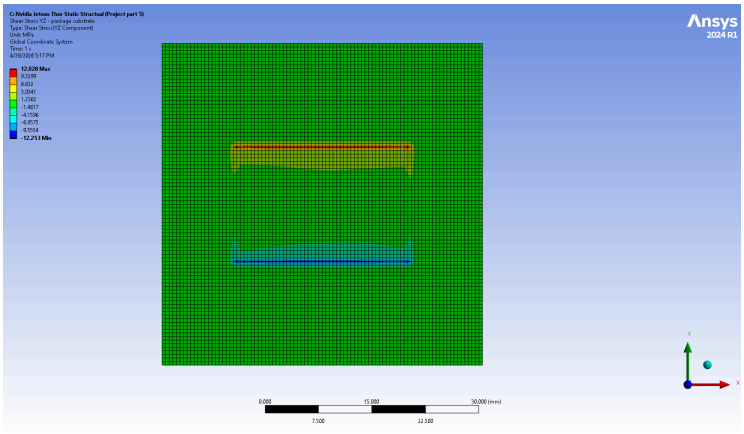
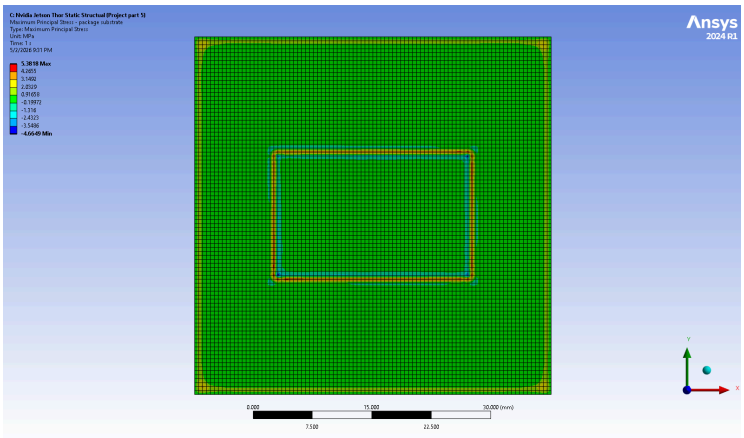
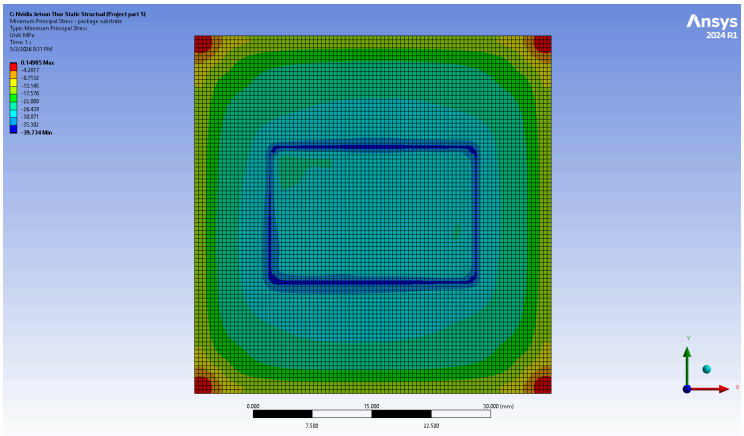
Layer	**Stress type**	**Image**
PCB	Normal σ_zz	
	Shear τ_xz	

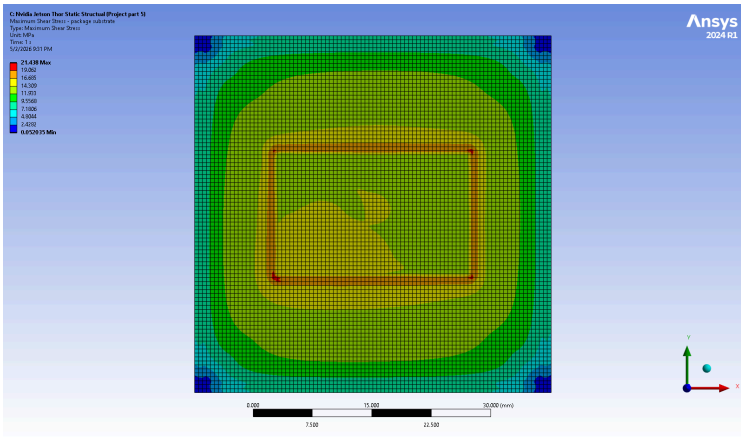
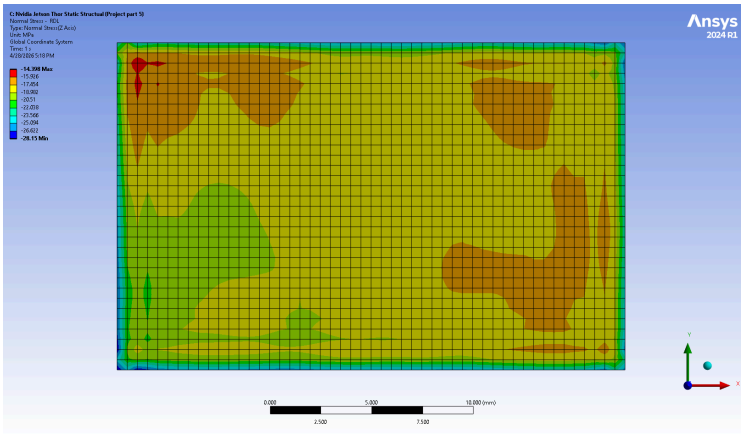
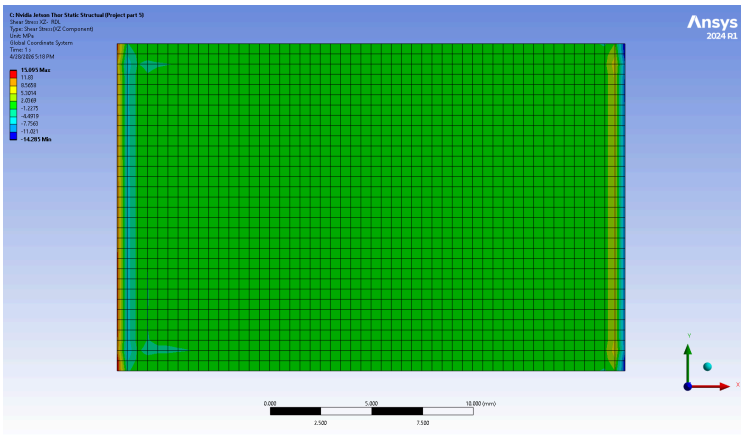
	Shear τ_yz	
	Maximum Principal σ_1	
	Minimum Principal σ_3	

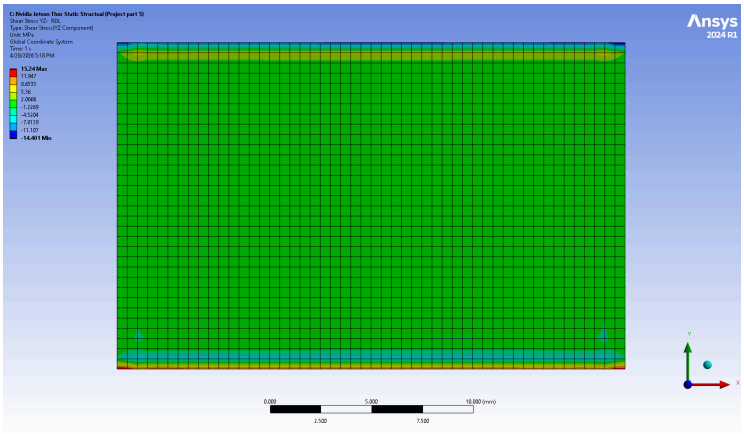
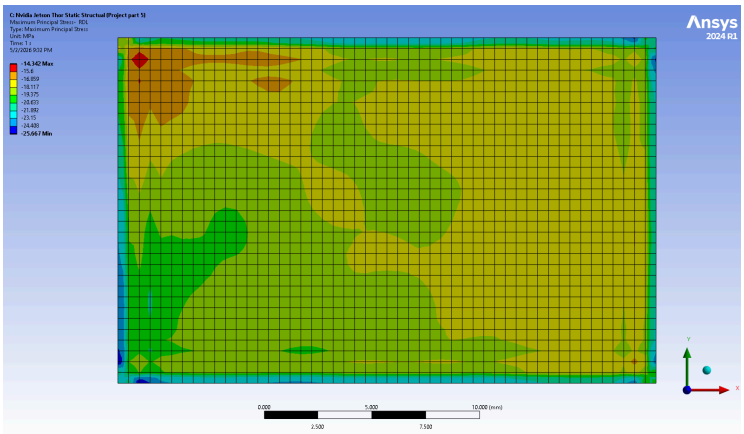
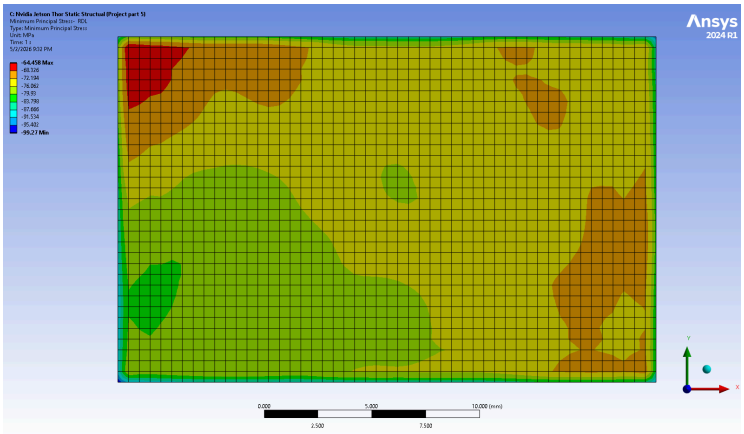
	Maximum Shear τ	
BGA	Normal σ_zz	
	Shear τ_xz	

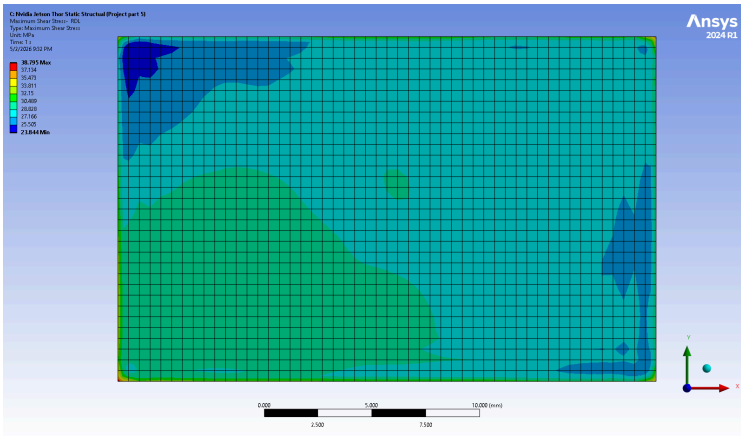
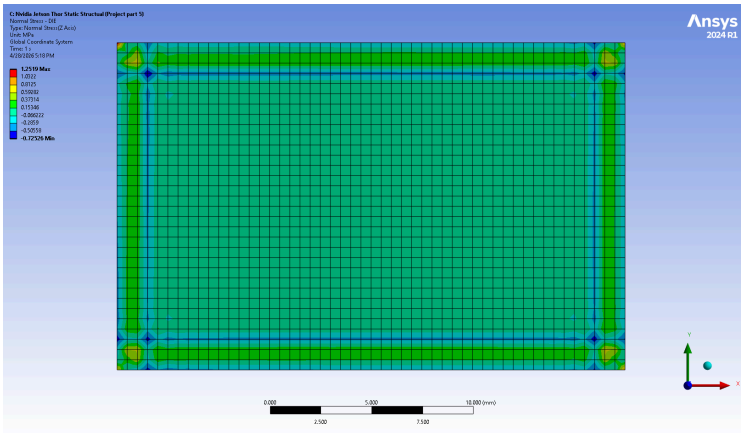
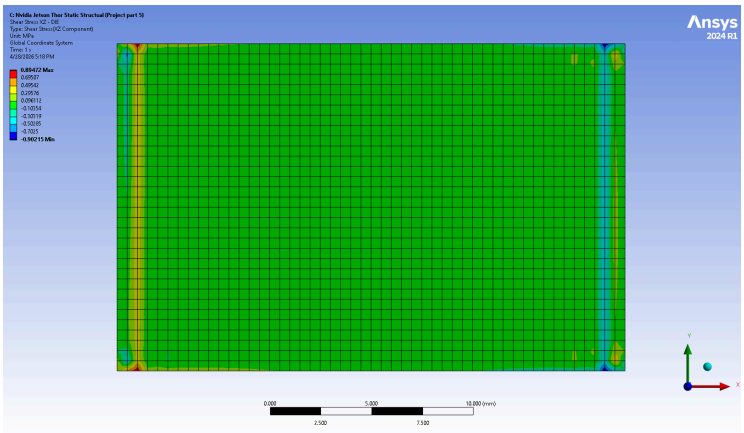
	Shear τ_yz	
	Maximum Principal σ_1	
	Minimum Principal σ_3	

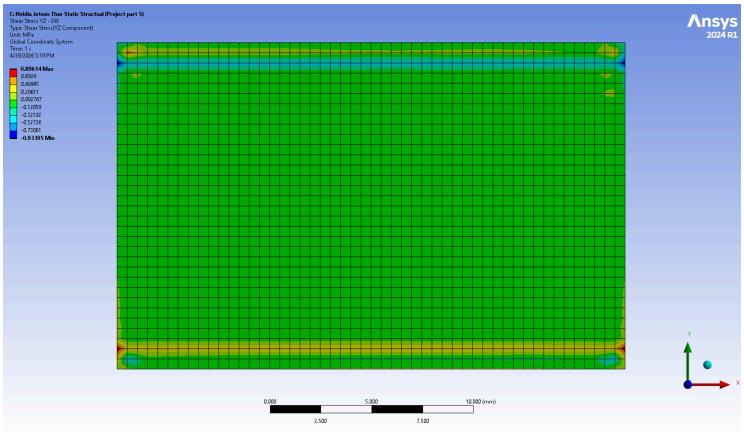
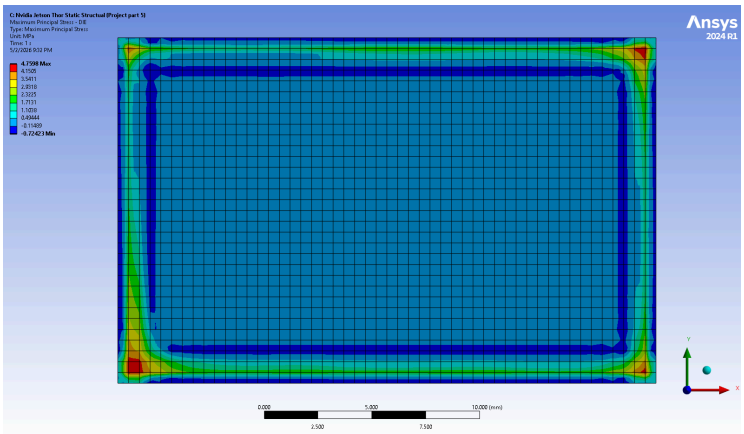
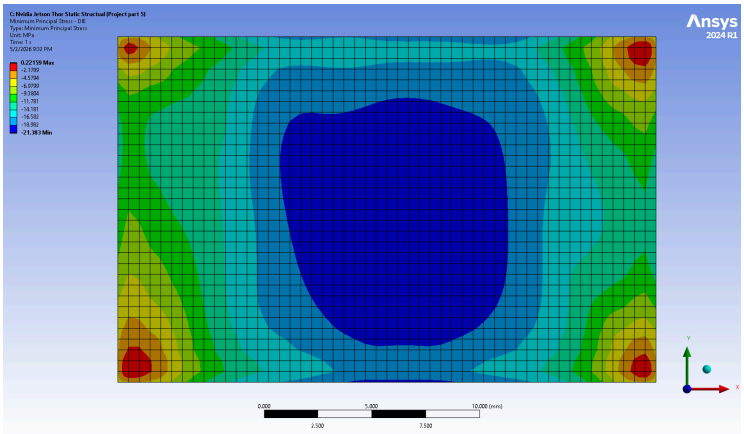
	Maximum Shear τ	
Package Substrate	Normal σ_zz	
	Shear τ_xz	

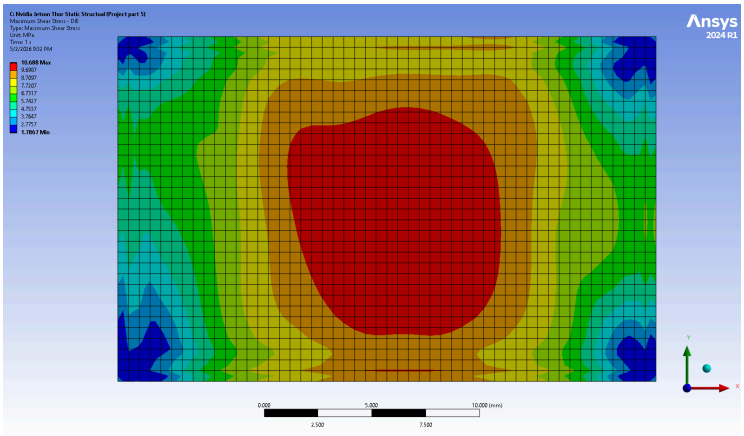
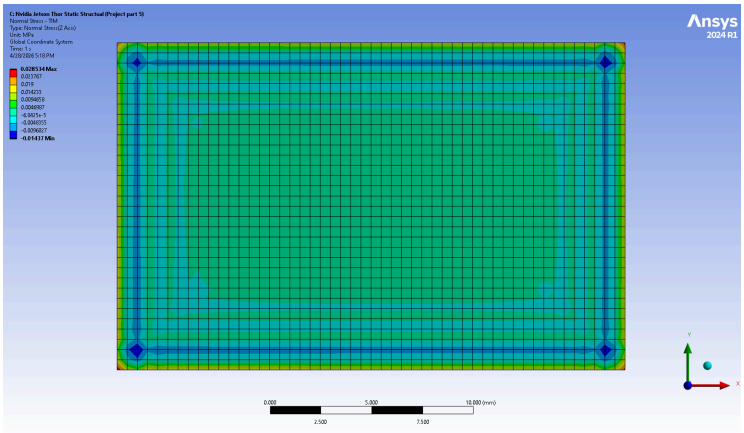
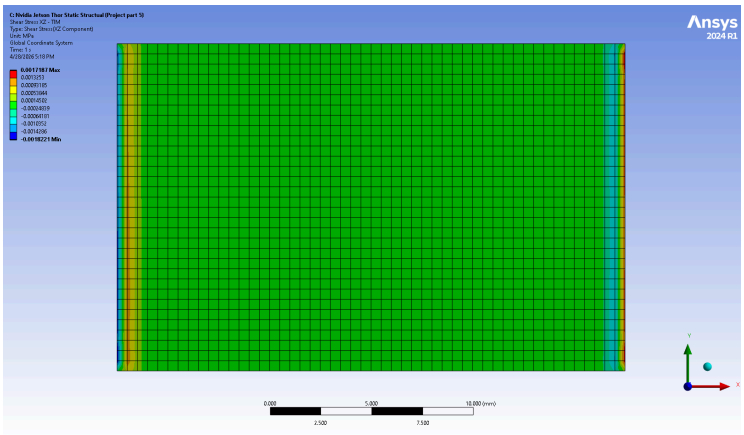
	Shear τ_yz	
	Maximum Principal σ_1	
	Minimum Principal σ_3	

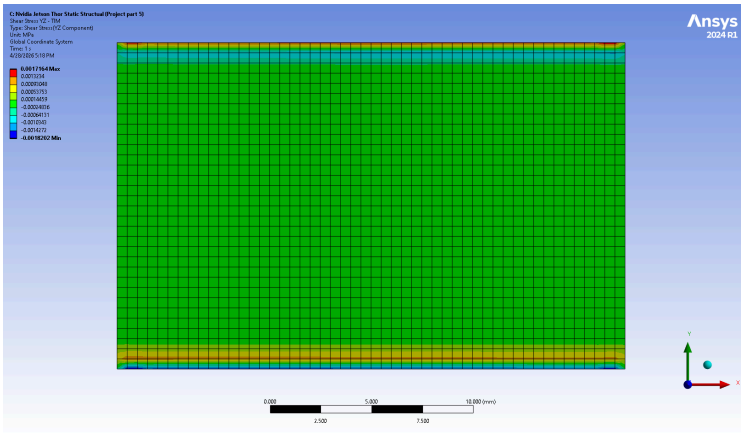
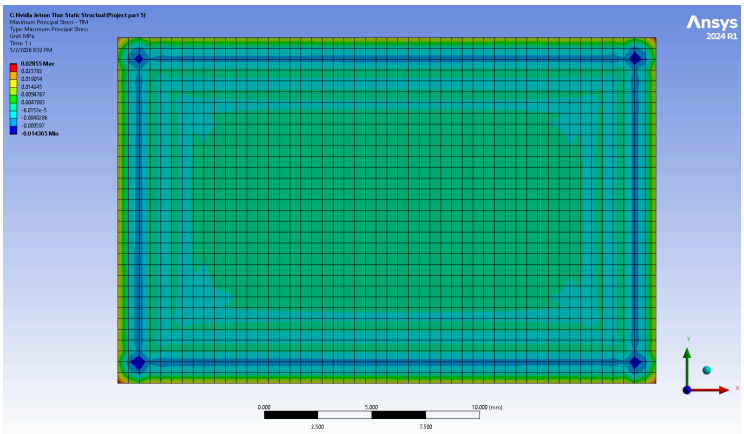
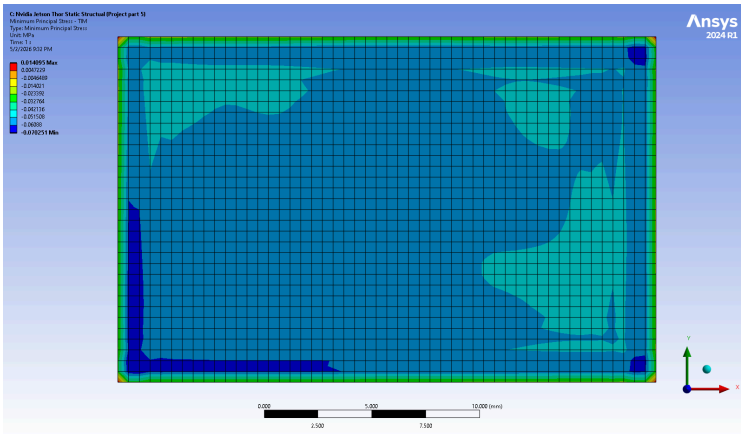
	Maximum Shear τ	
RDL	Normal σ_zz	
	Shear τ_xz	

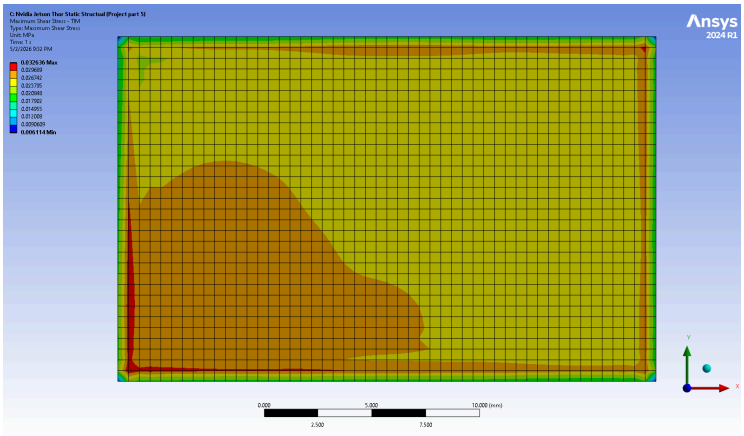
	Shear τ_yz	
	Maximum Principal σ_1	
	Minimum Principal σ_3	

	Maximum Shear τ	
DIE	Normal σ_zz	
	Shear τ_xz	

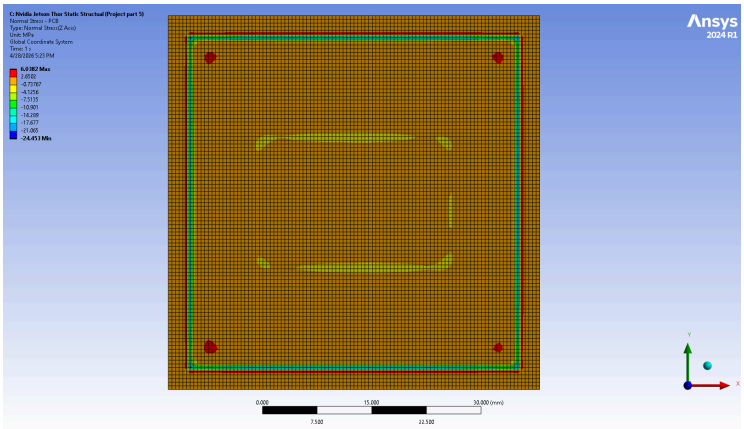
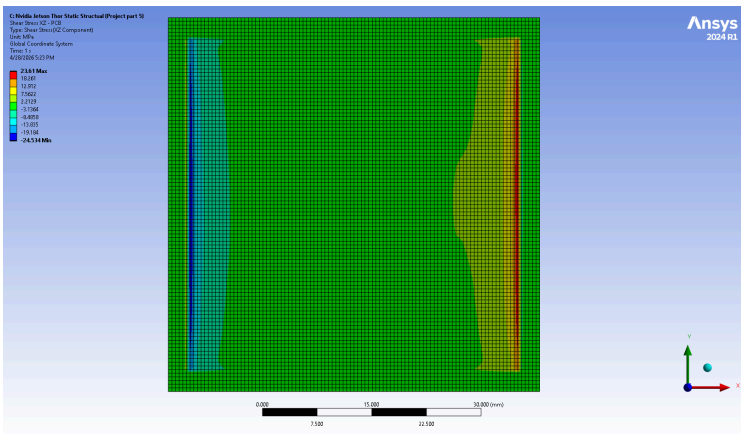
	Shear τ_yz	
	Maximum Principal σ_1	
	Minimum Principal σ_3	

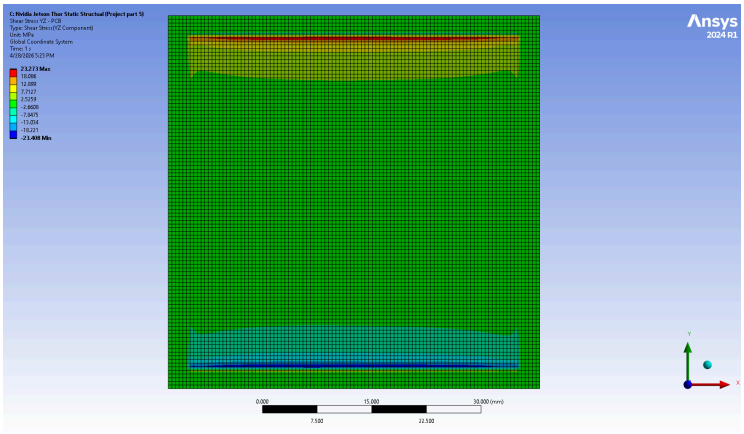
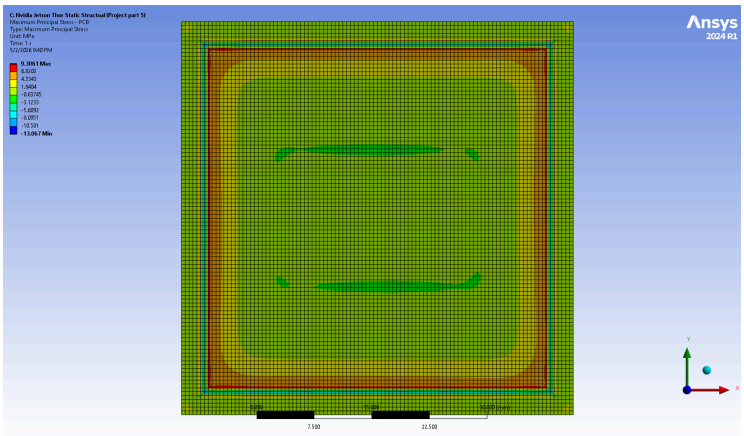
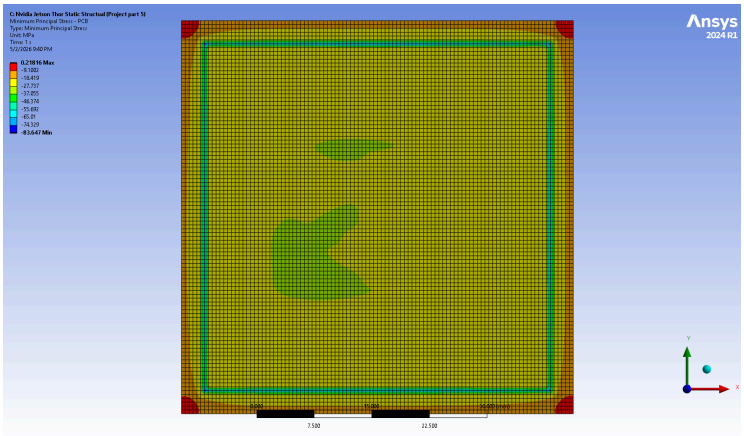
	Maximum Shear τ	
TIM	Normal σ_zz	
	Shear τ_xz	

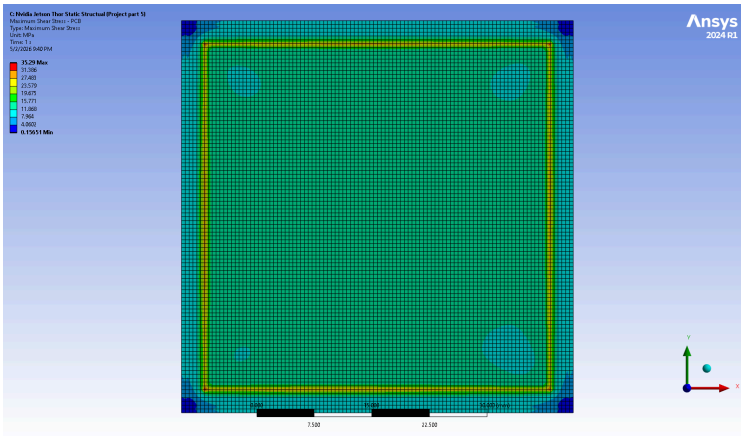
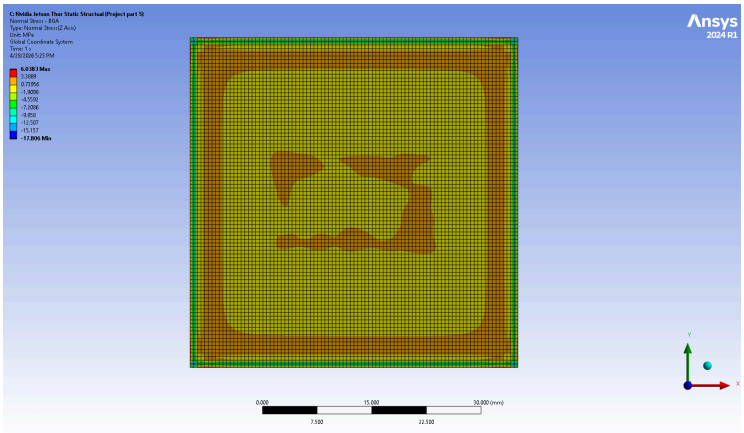
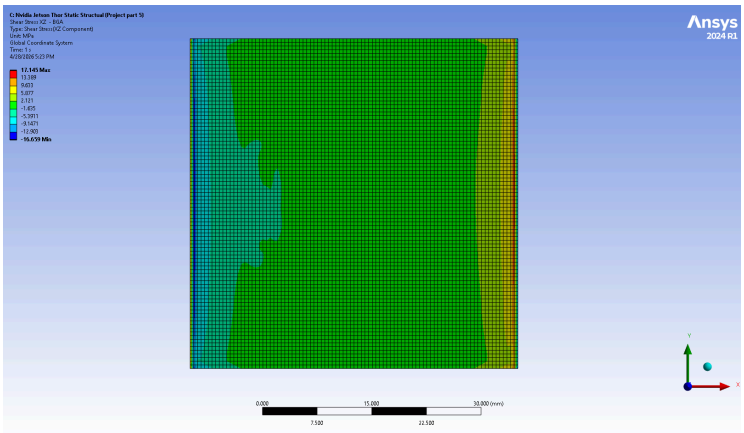
	Shear τ_yz	
	Maximum Principal σ_1	
	Minimum Principal σ_3	

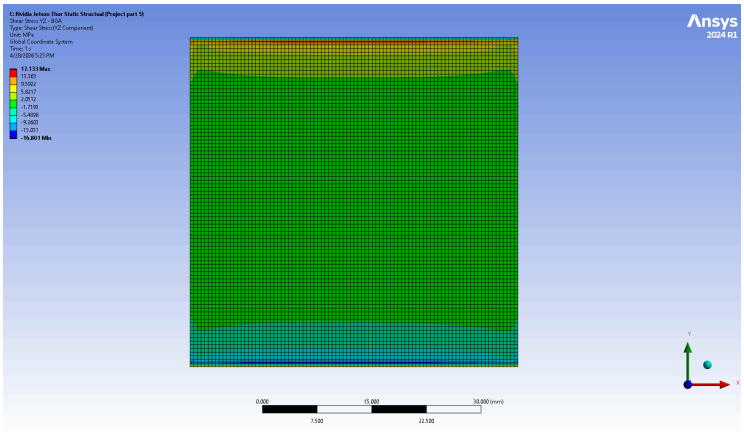
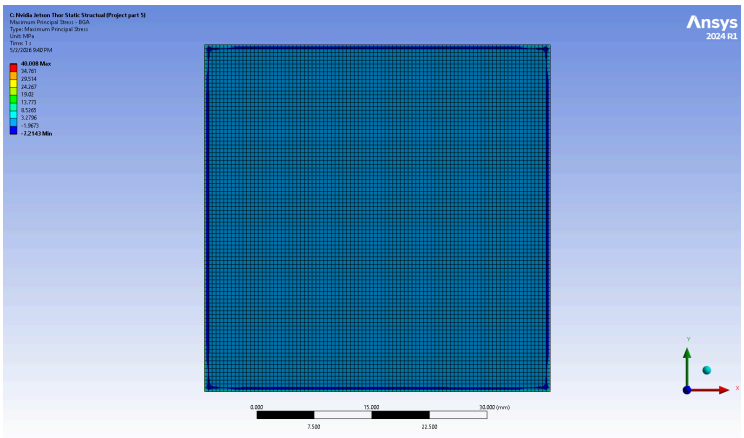
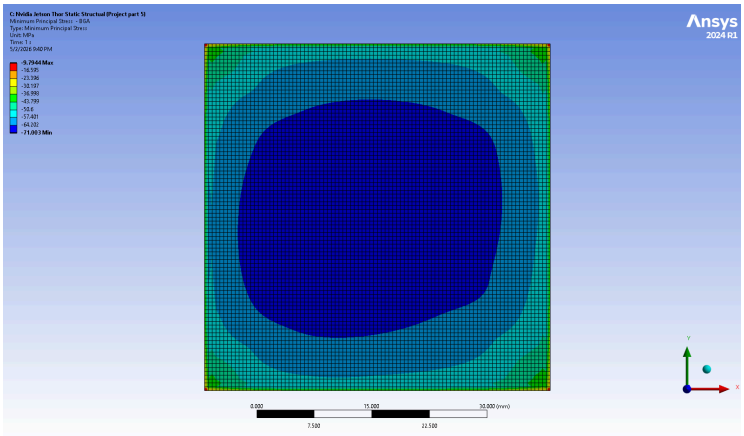
	Maximum Shear τ	

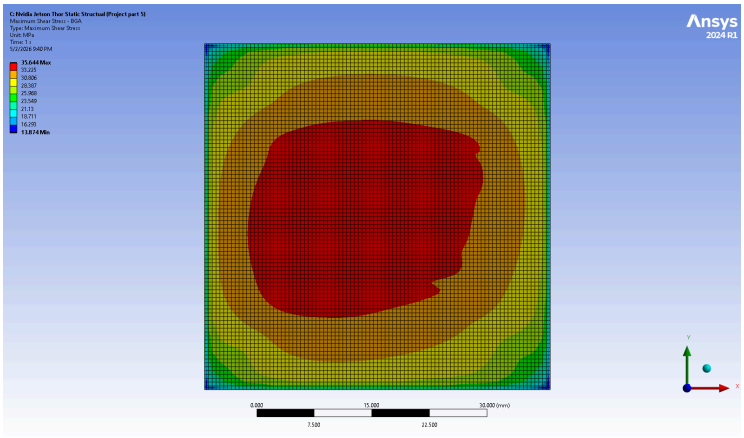
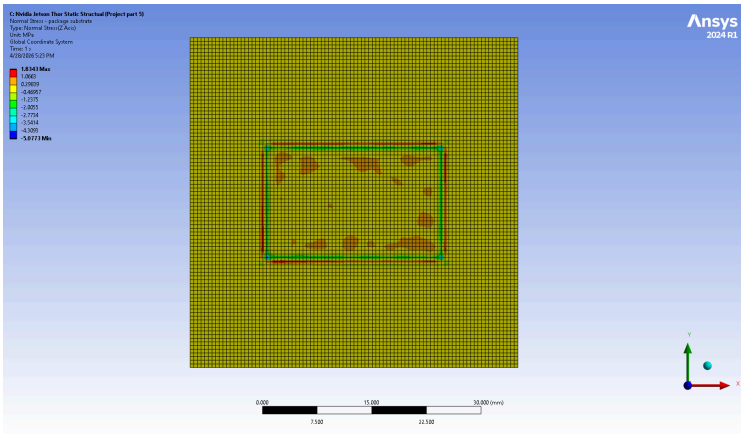
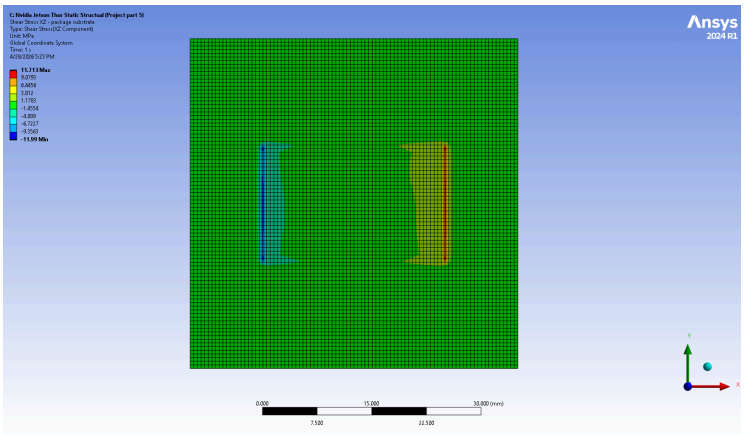
[12] Table 9: Stress results for across every device layer for powermap 3:

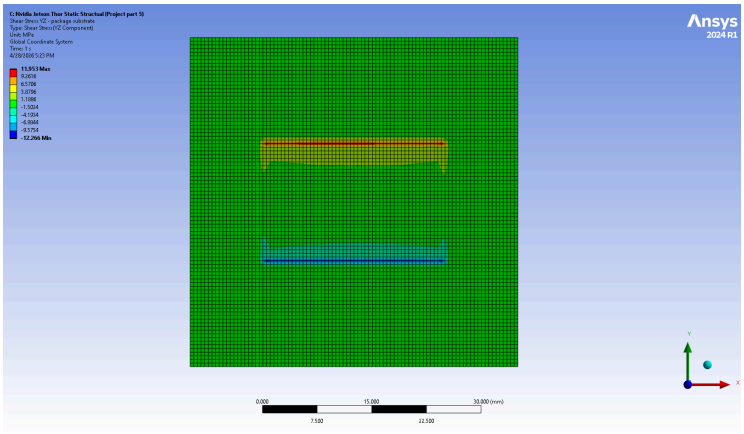
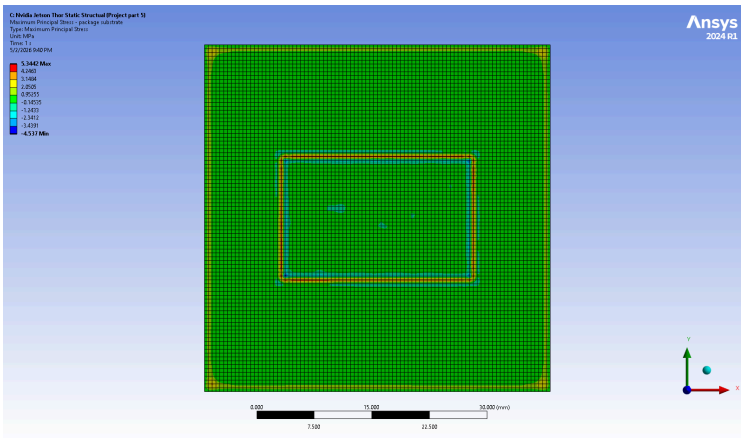
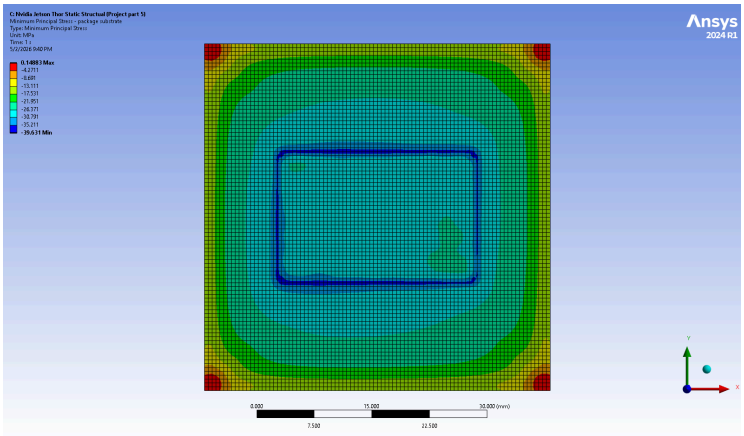
Layer	**Stress type**	**Image**
PCB	Normal σ_zz	
	Shear τ_xz	

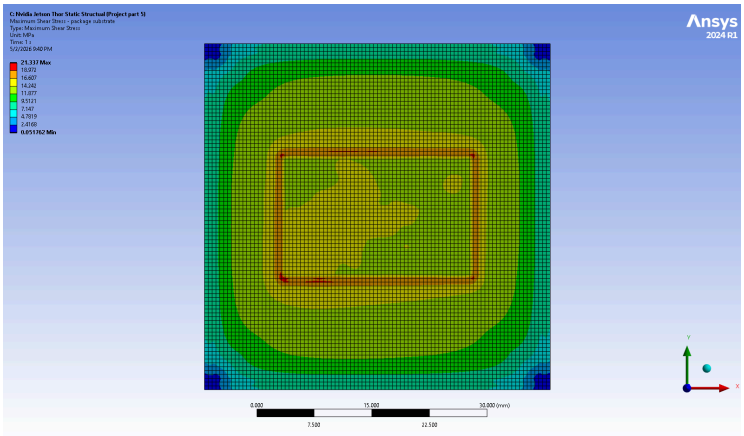
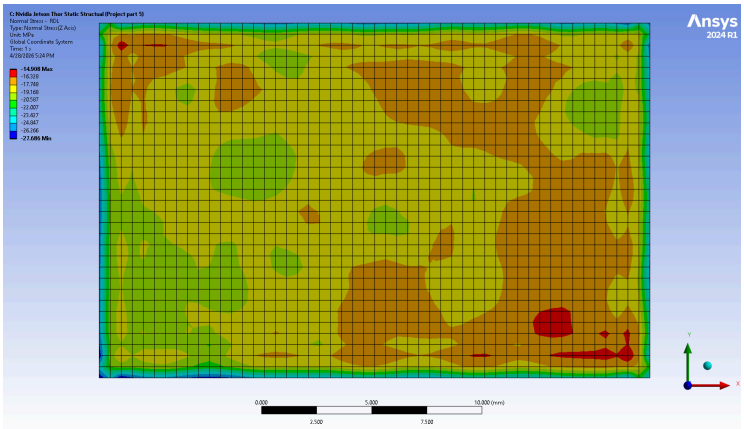
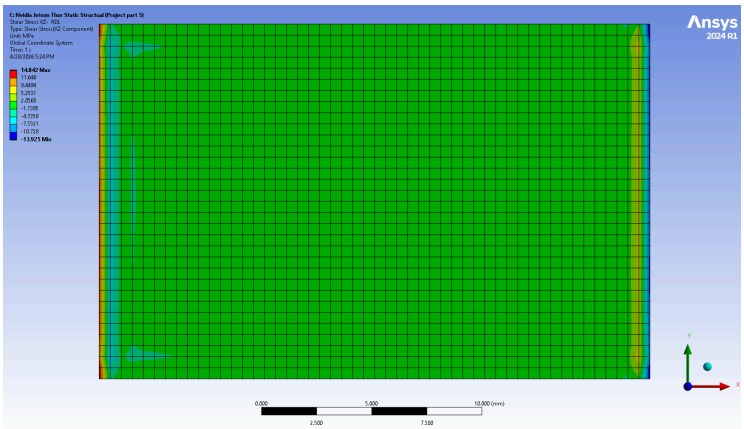
	Shear τ_yz	
	Maximum Principal σ_1	
	Minimum Principal σ_3	

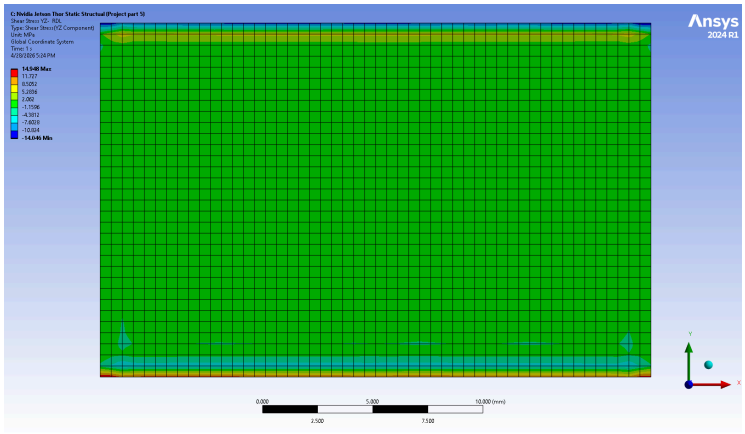
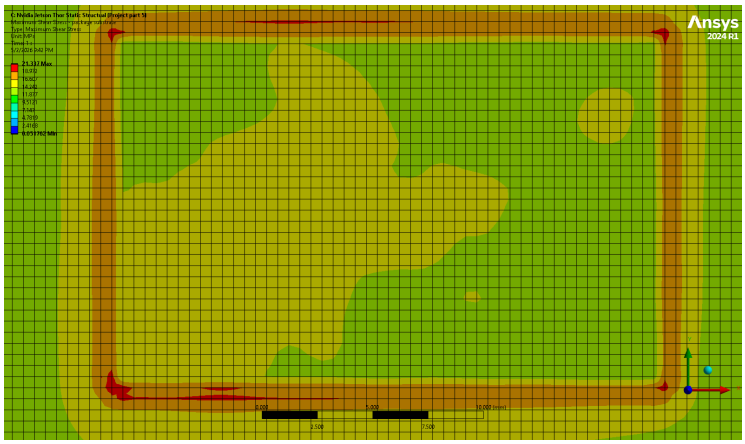
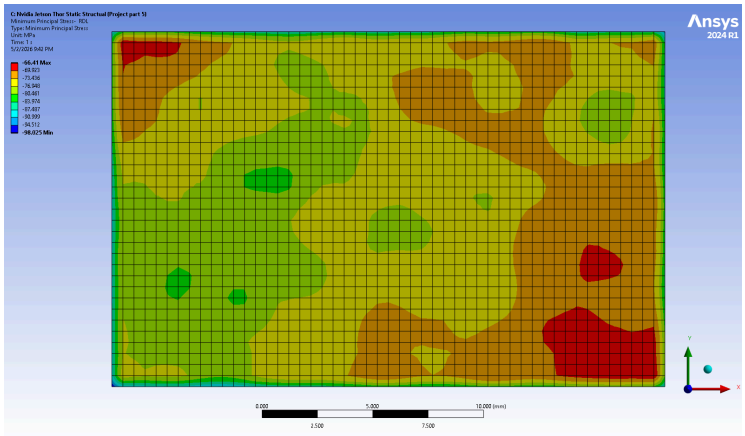
	Maximum Shear τ	
BGA	Normal σ_zz	
	Shear τ_xz	

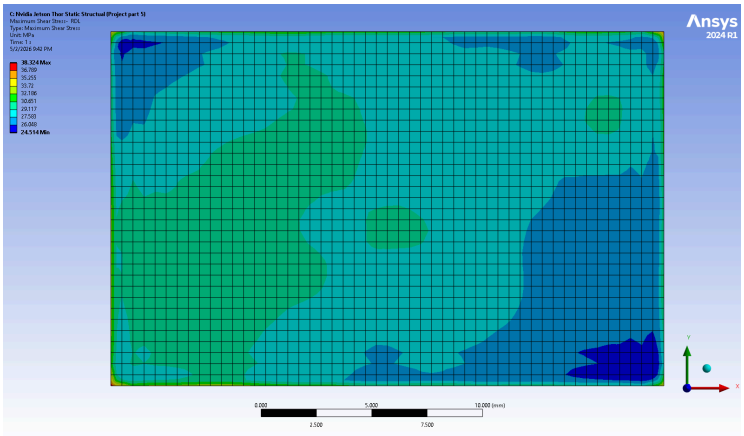
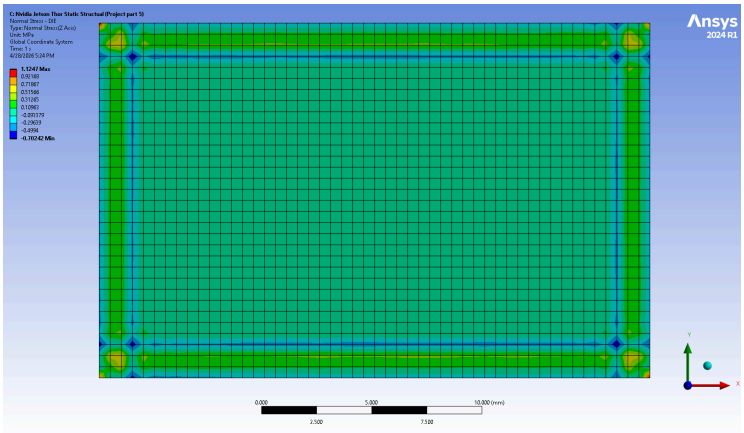
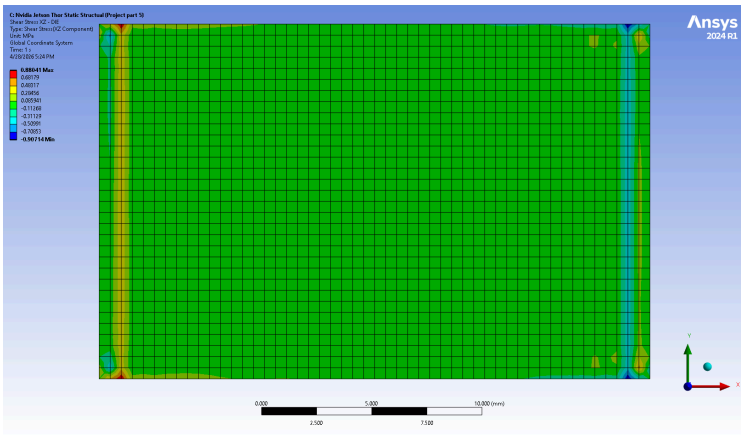
	Shear τ_yz	
	Maximum Principal σ_1	
	Minimum Principal σ_3	

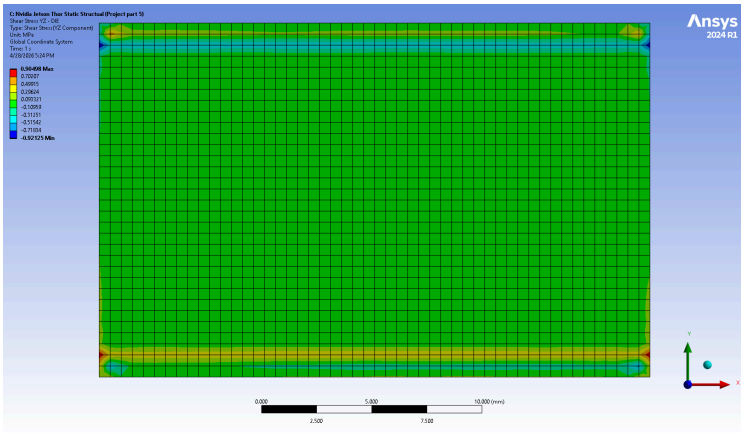
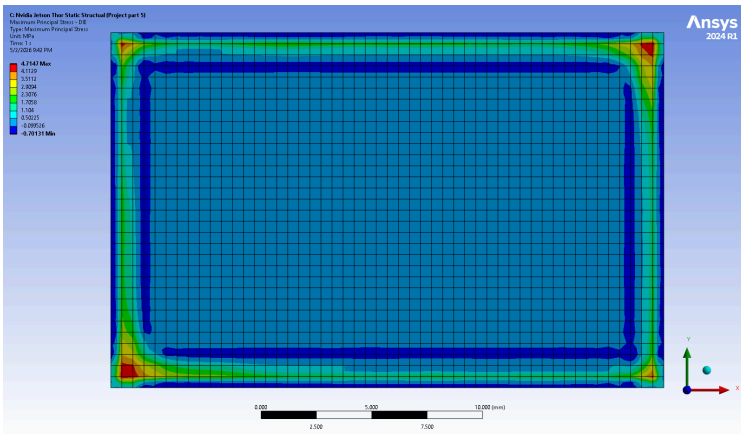
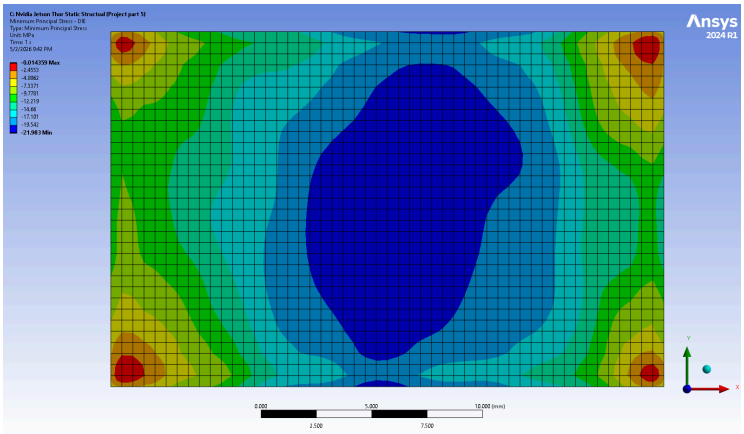
	Maximum Shear τ	
Package Substrate	Normal σ_zz	
	Shear τ_xz	

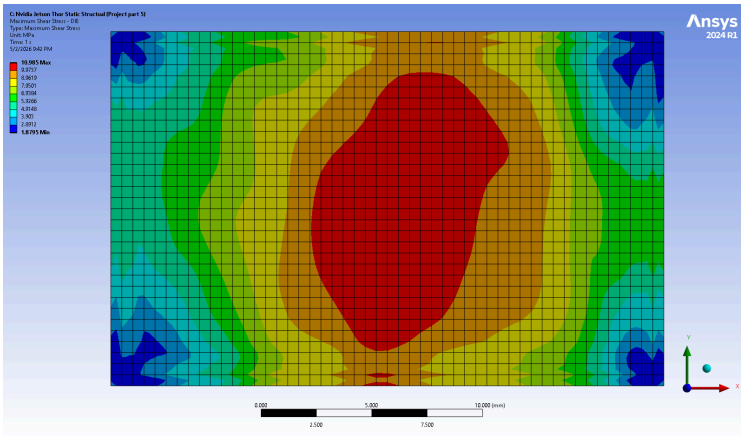
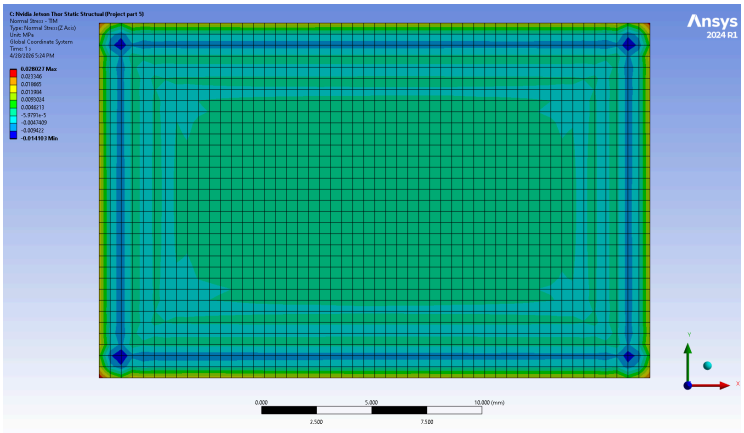
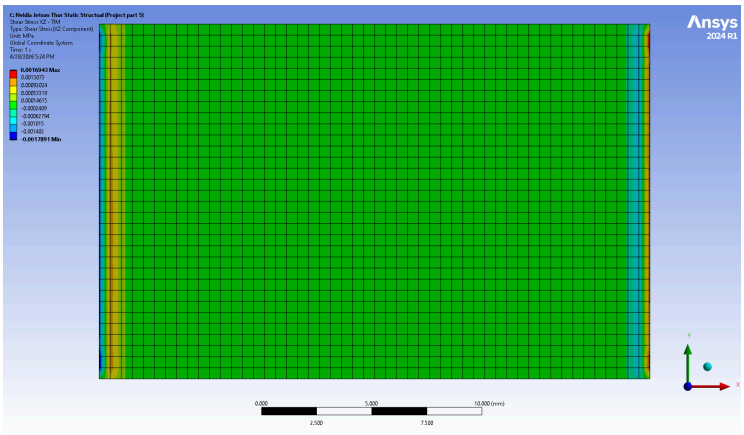
	Shear τ_yz	
	Maximum Principal σ_1	
	Minimum Principal σ_3	

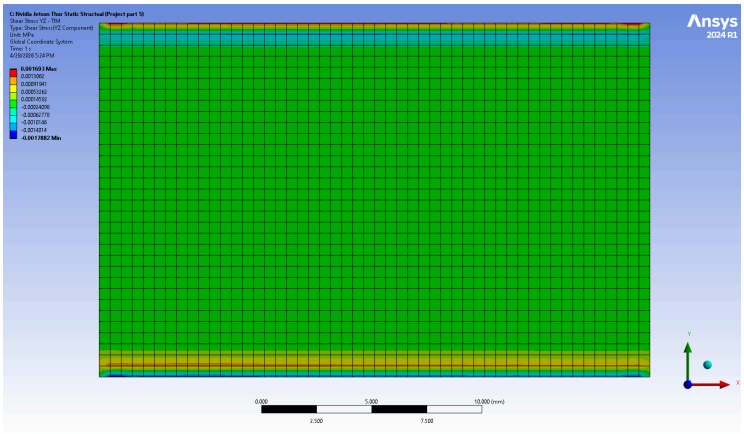
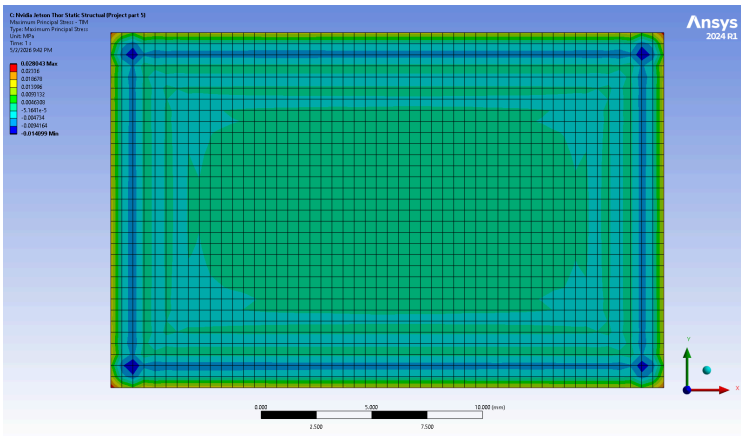
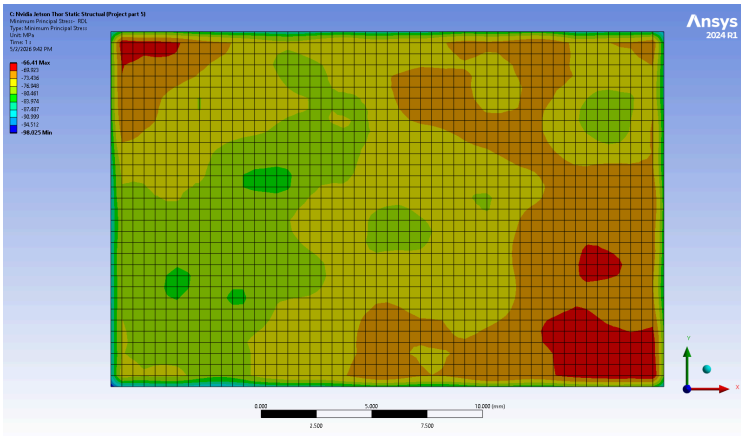
	Maximum Shear τ	
RDL	Normal σ_zz	
	Shear τ_xz	

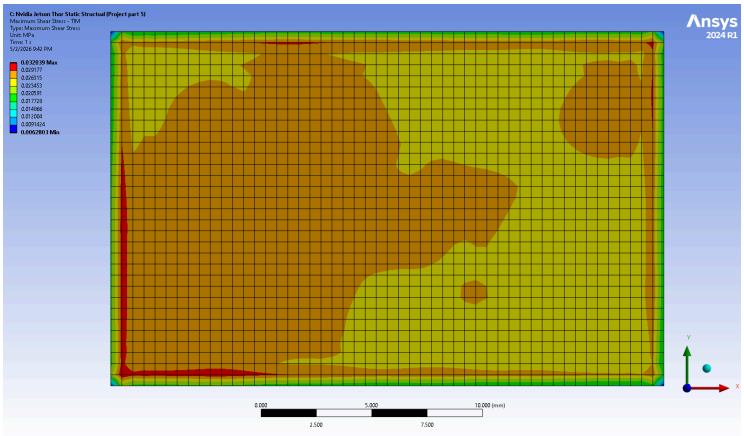
	Shear τ_yz	
	Maximum Principal σ_1	
	Minimum Principal σ_3	

	Maximum Shear τ	
DIE	Normal σ_zz	
	Shear τ_xz	

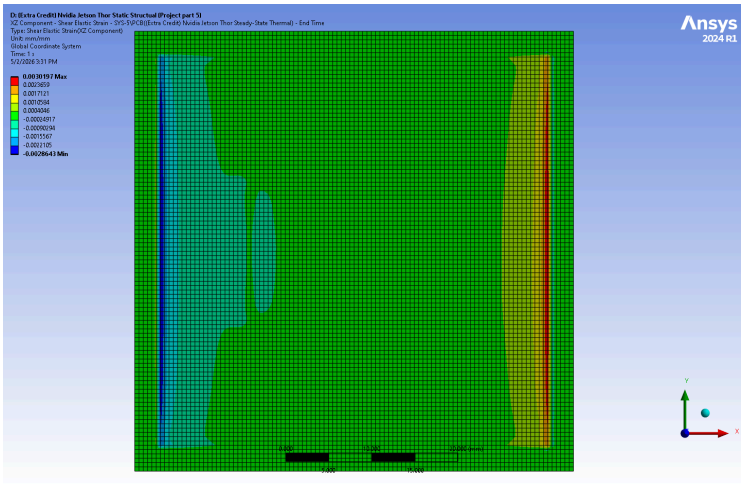
	Shear τ_yz	
	Maximum Principal σ_1	
	Minimum Principal σ_3	

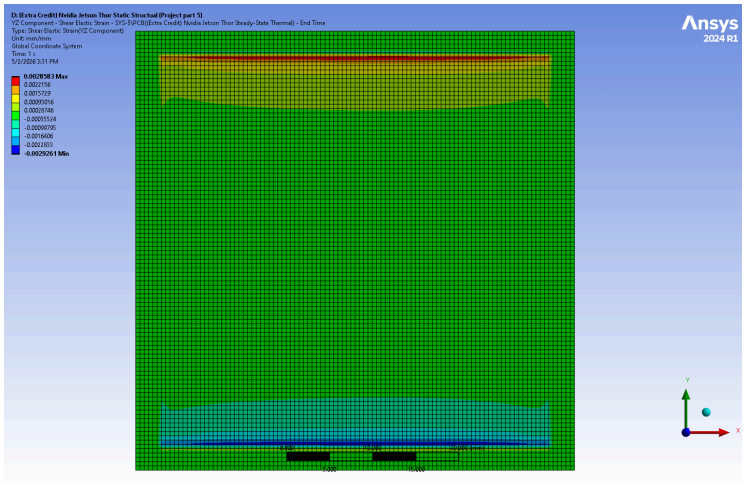
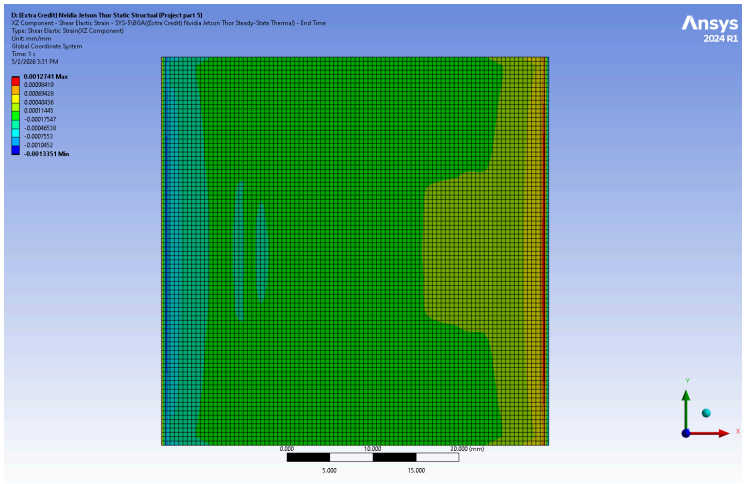
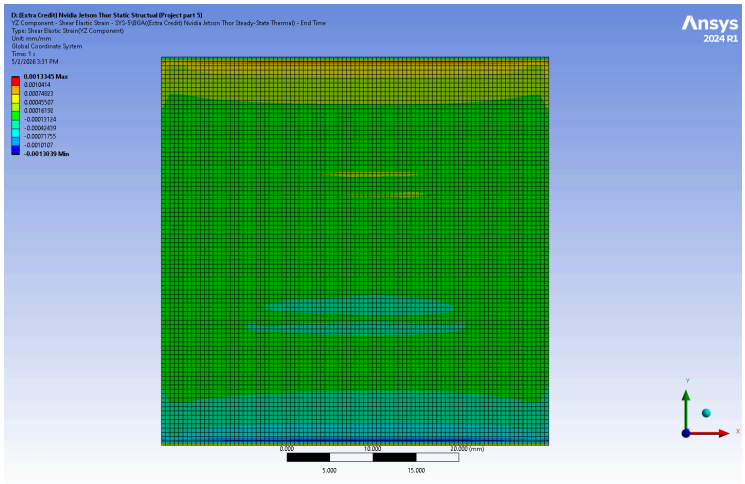
	Maximum Shear τ	
TIM	Normal σ_zz	
	Shear τ_xz	

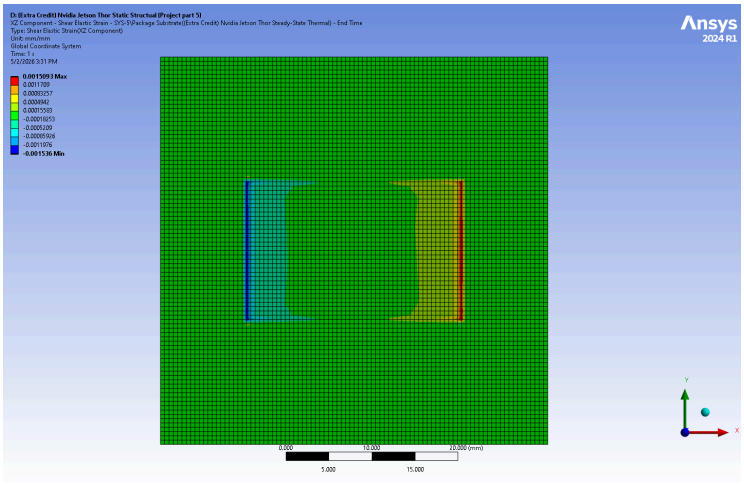
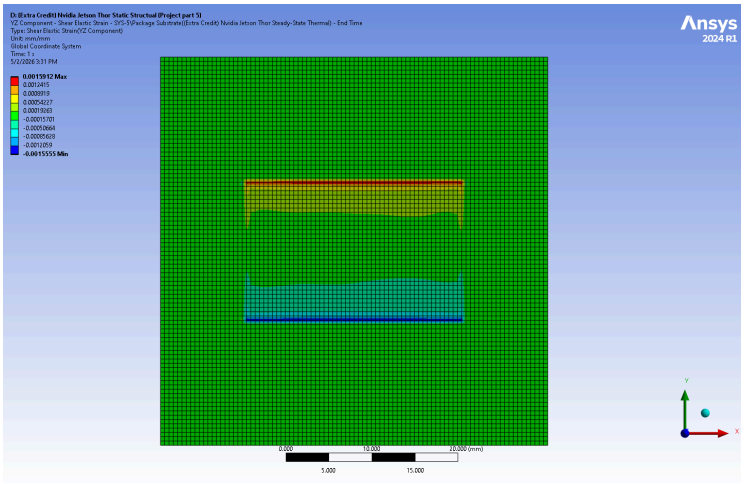
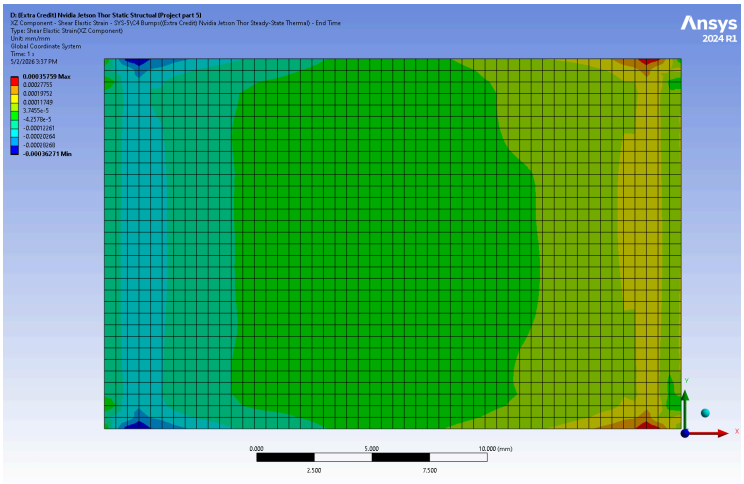
	Shear τ_yz	
	Maximum Principal σ_1	
	Minimum Principal σ_3	

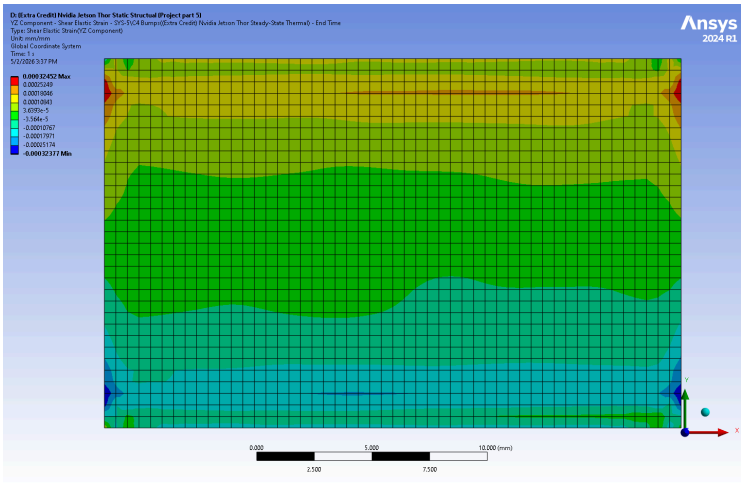
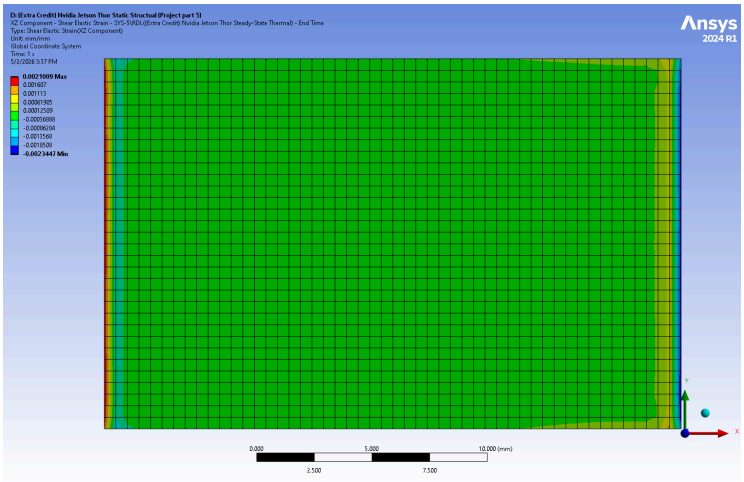
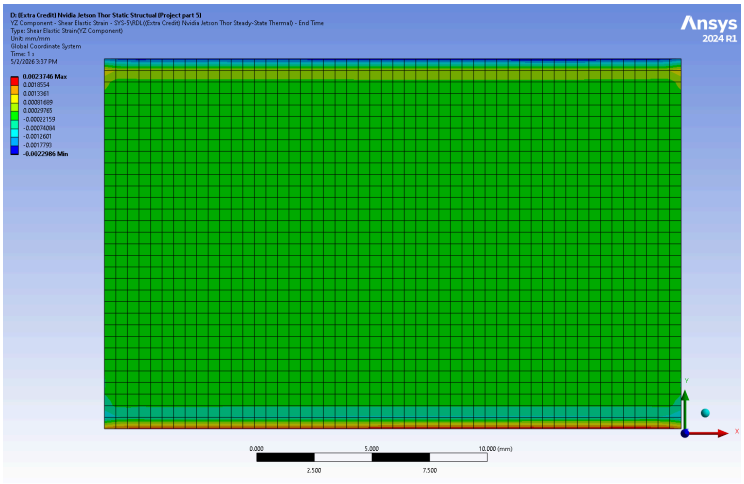
	Maximum Shear τ	

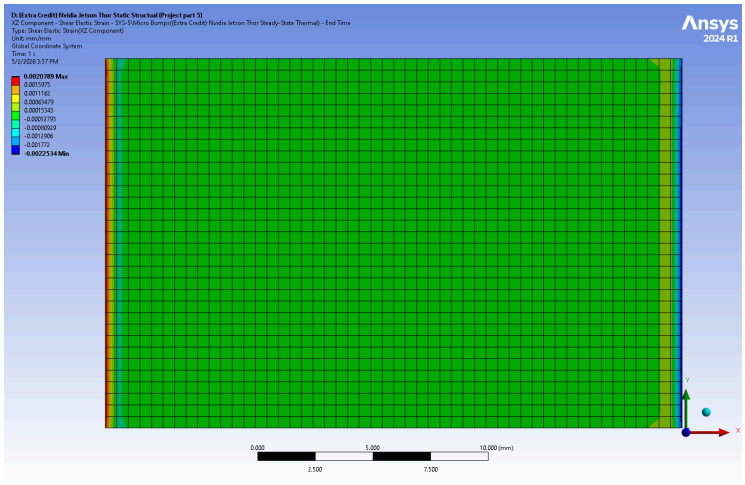
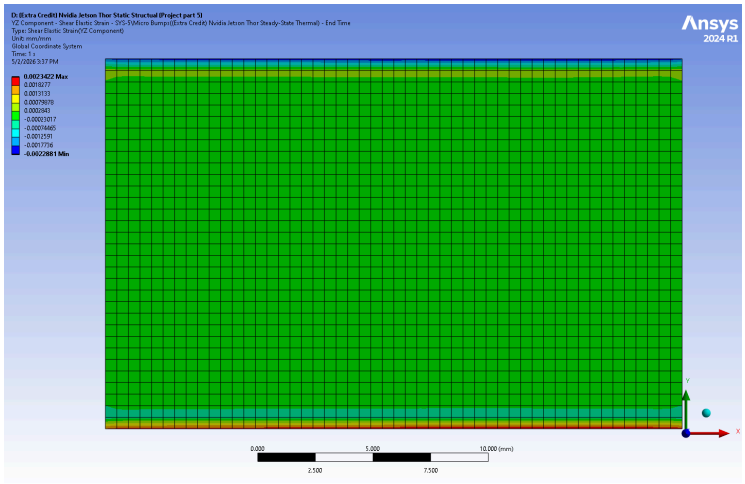
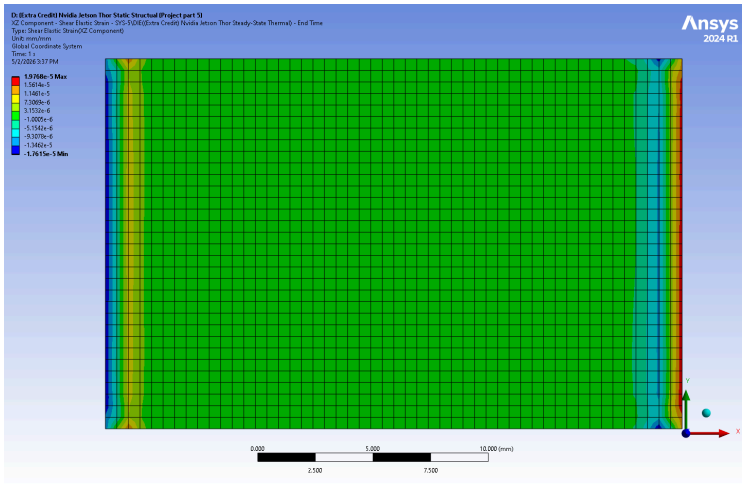
[13] Table 11: Strain results across every device layer for powermap 1, now including C4 Bumps and Micro Bumps layers:

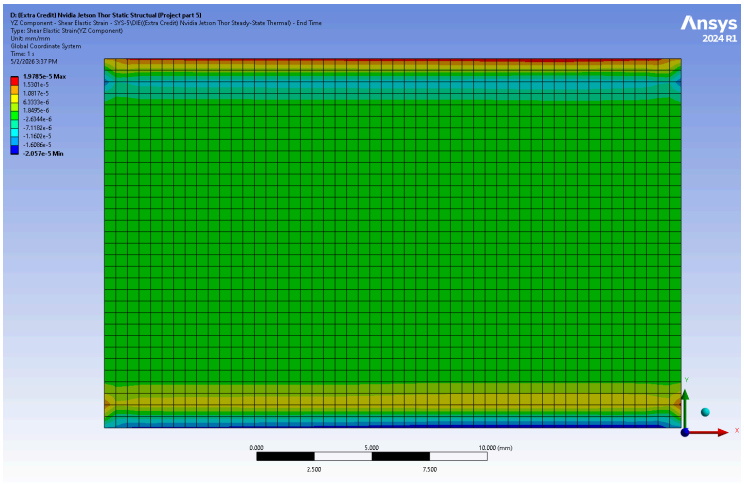
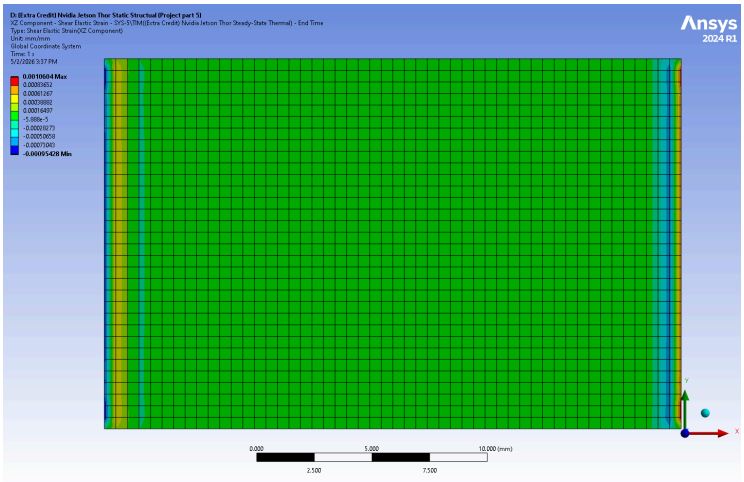
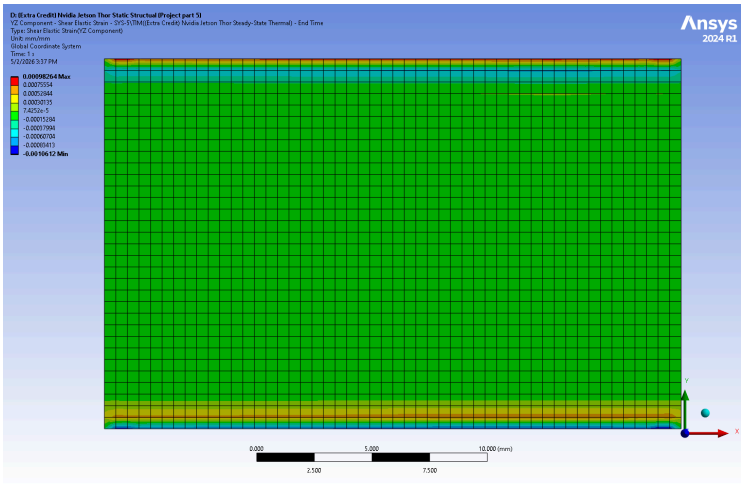
Layer	**Strain type**	**Image**
PCB	Strain τ_xz	

	Strain τ_yz	
BGA	Strain γ_xz	
	Strain γ_yz	

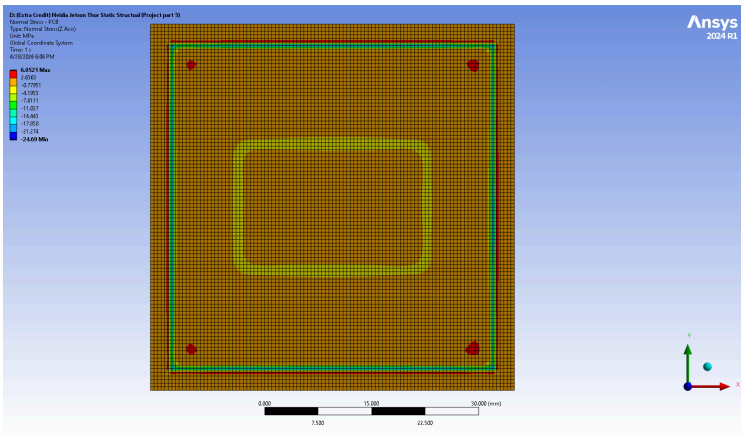
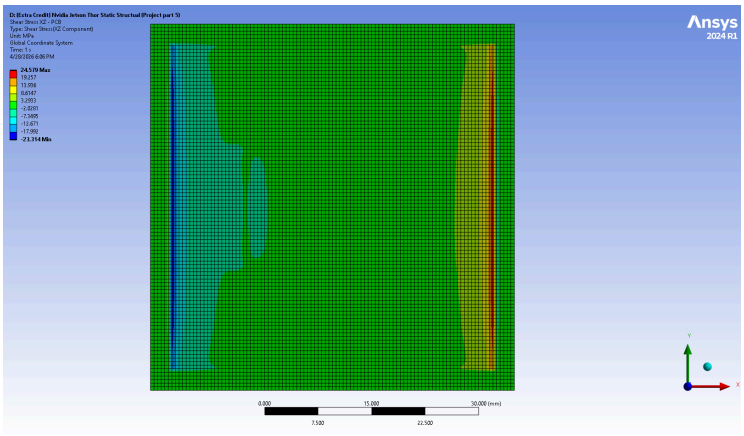
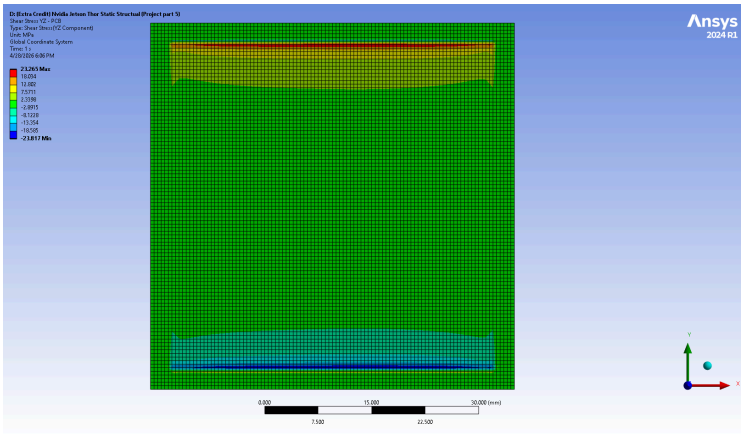
Package Substrate	Strain γ_xz	
	Strain γ_yz	
C4 Bumps	Strain γ_xz	

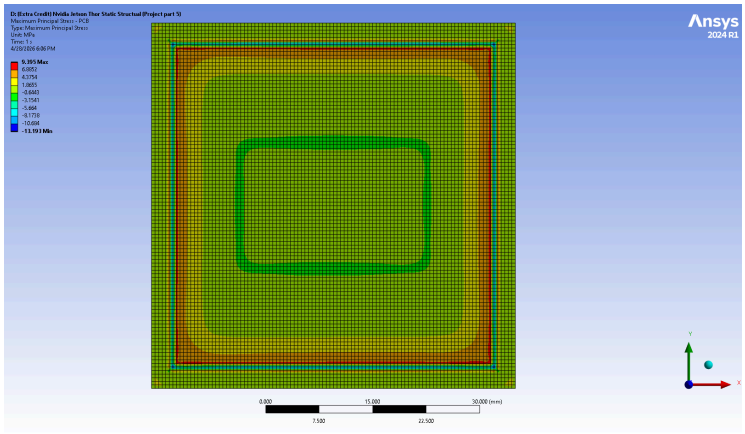
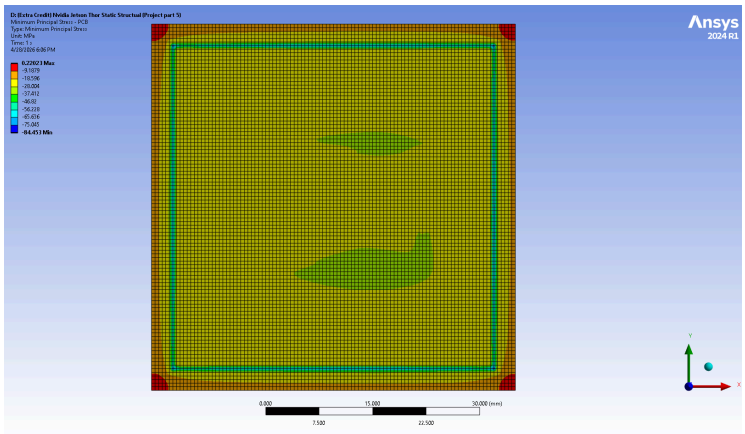
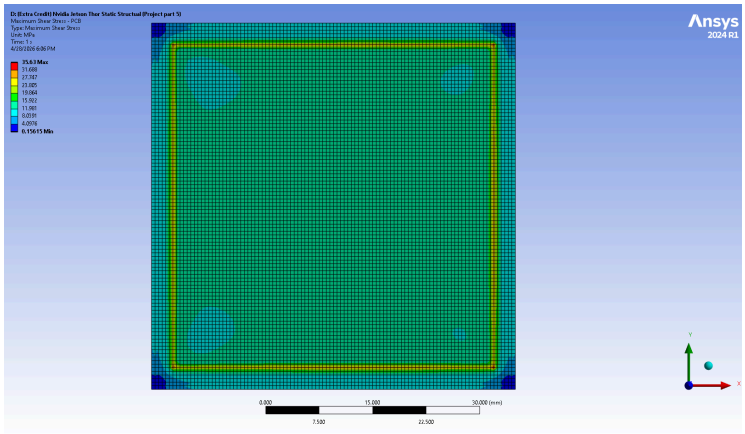
	Strain γ_yz	
RDL	Strain γ_xz	
	Strain γ_yz	

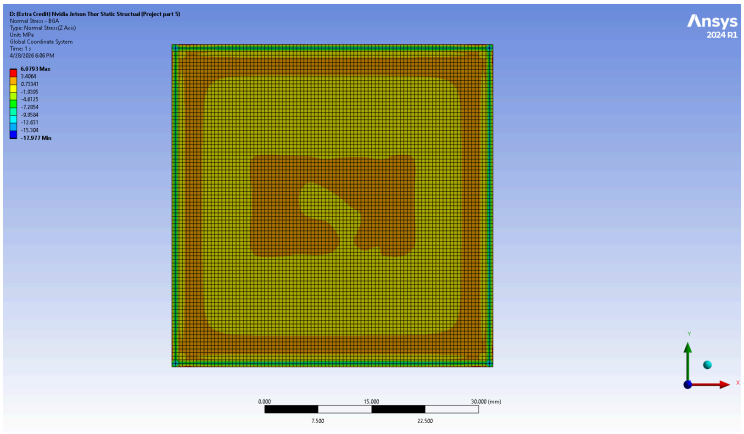
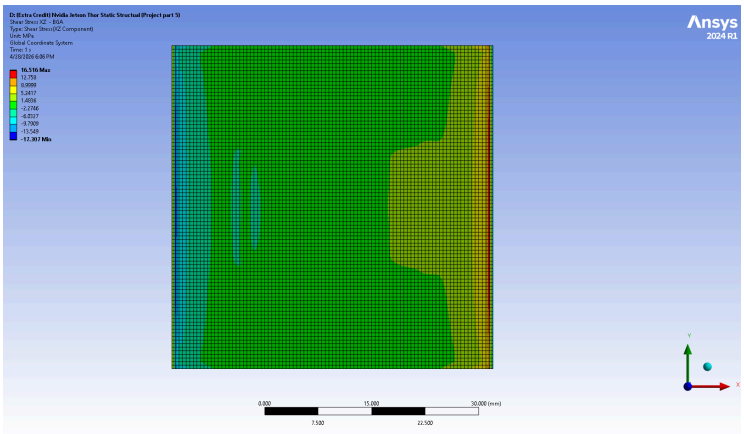
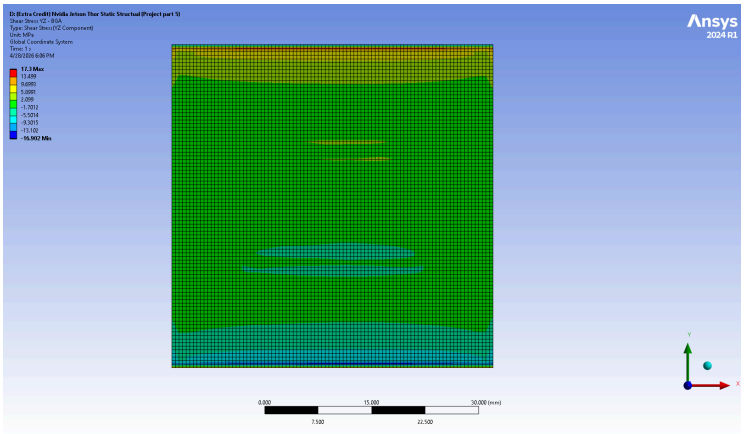
Micro Bumps	Strain γ_xz	
	Strain γ_yz	
Die	Shear γ_xz	

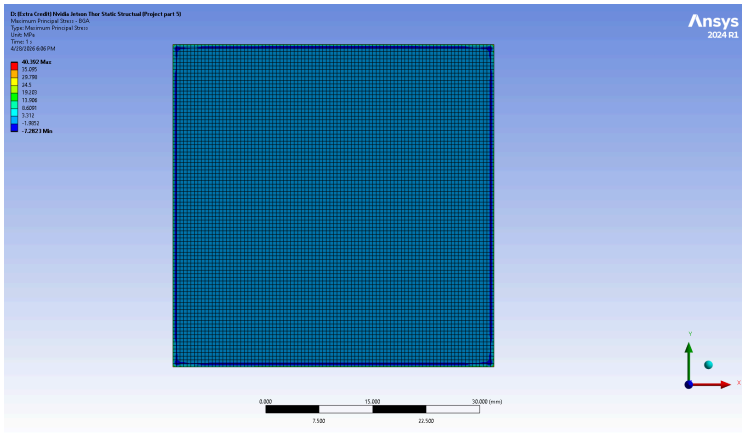
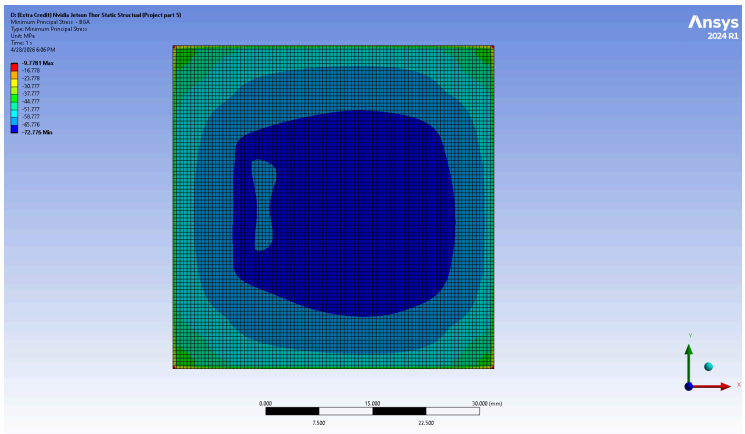
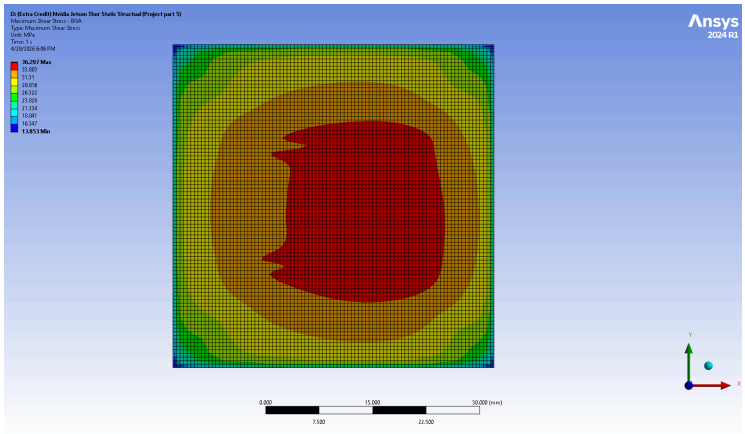
	Shear γ_yz	
TIM	Shear γ_xz	
	Shear γ_yz	

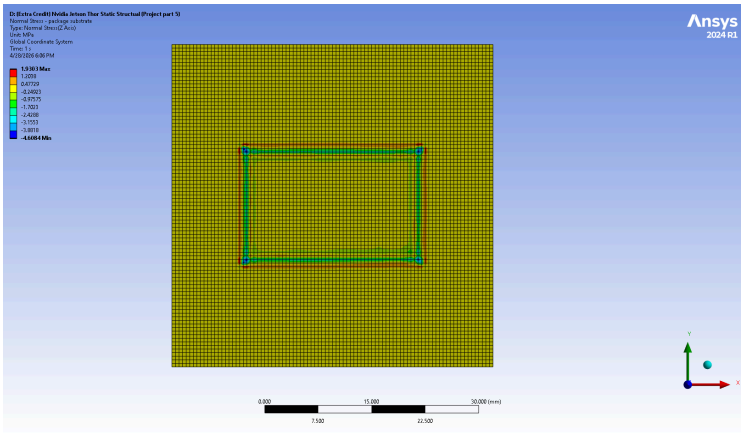
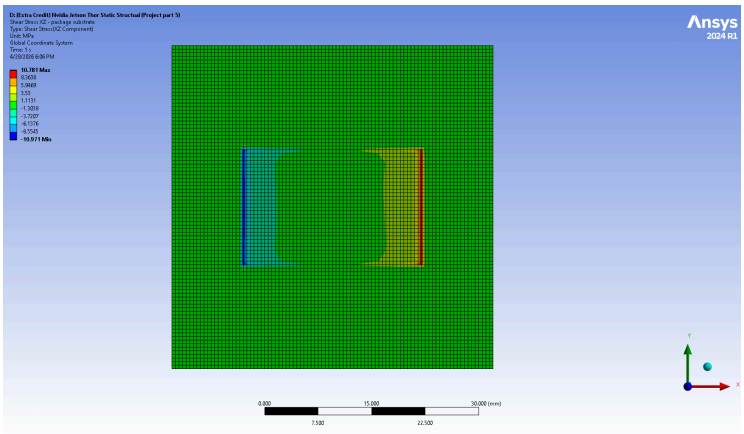
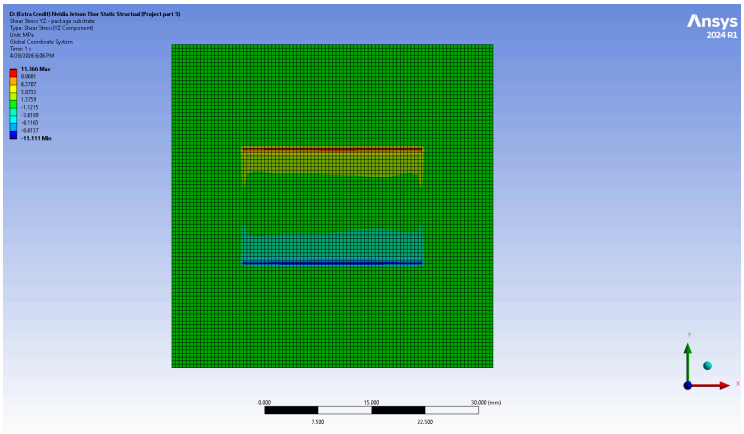
[14] Table 12: Stress results for across every device layer for powermap 1, now including C4 Bumps and Micro Bumps layers:

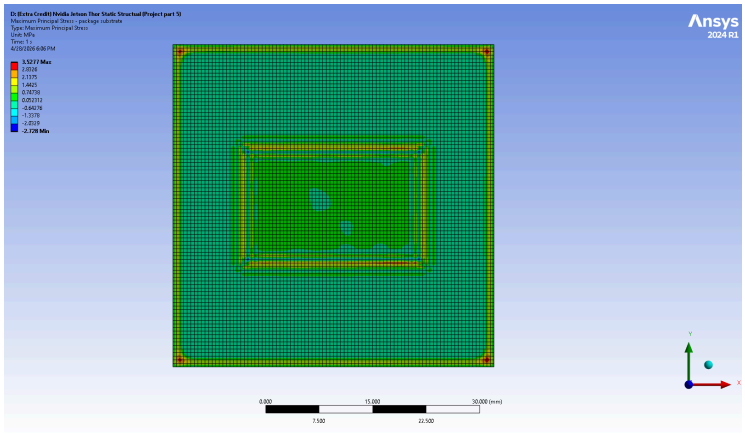
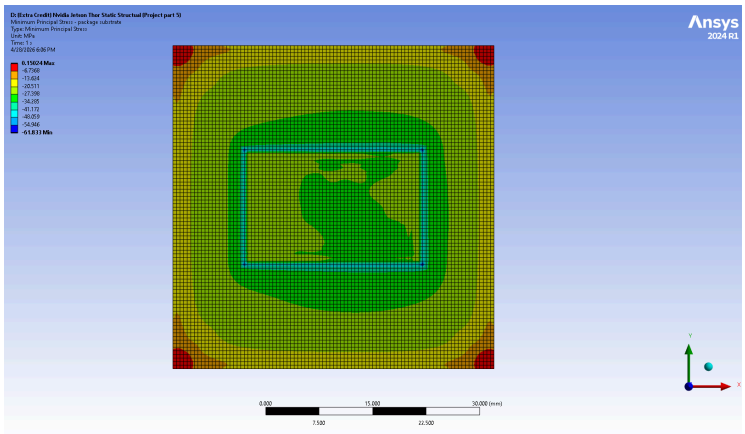
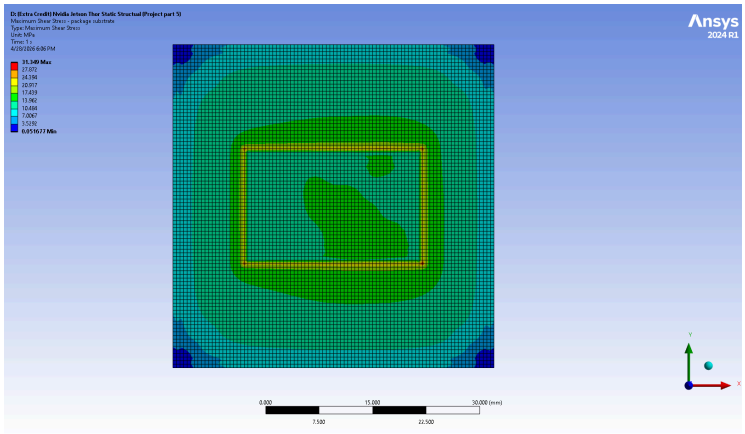
Layer	Stress type	Image
PCB	Normal σ_zz	
	Shear τ_xz	
	Shear τ_yz	

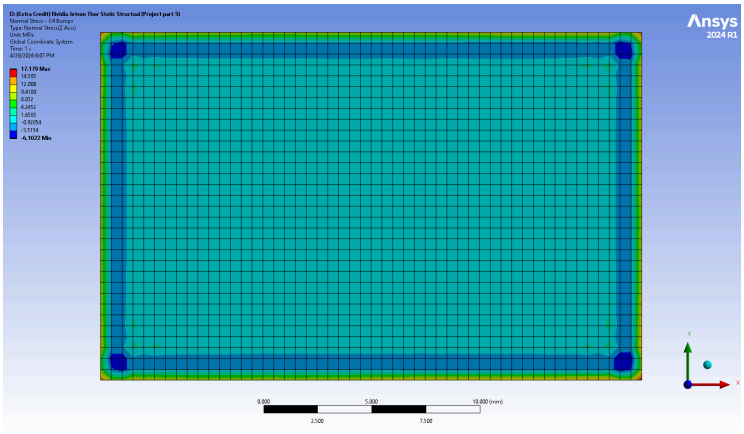
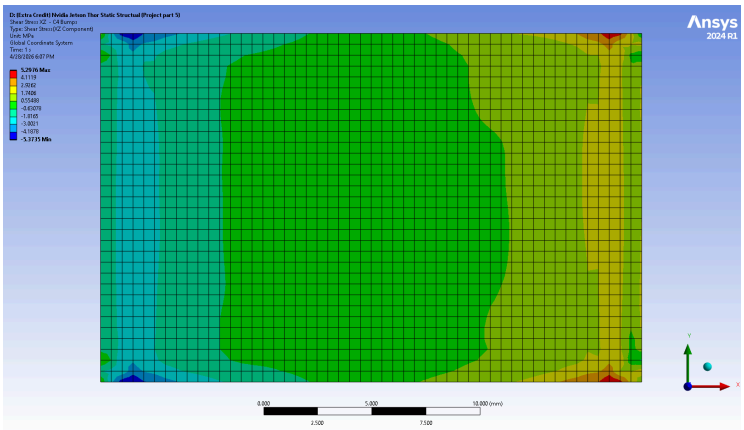
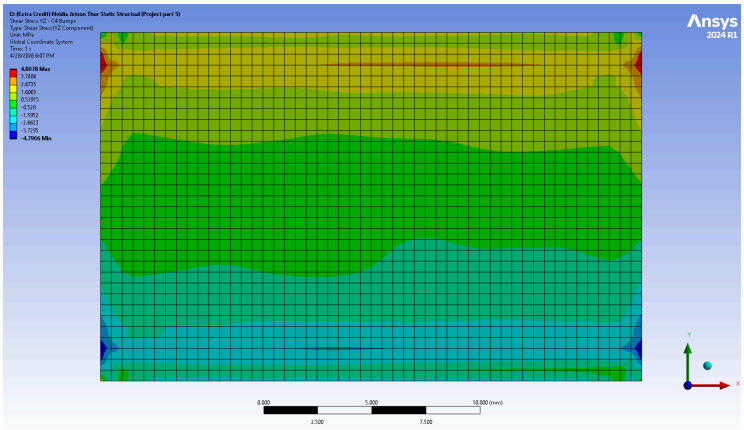
	Maximum Principal σ_1	
	Minimum Principal σ_3	
	Maximum Shear τ	

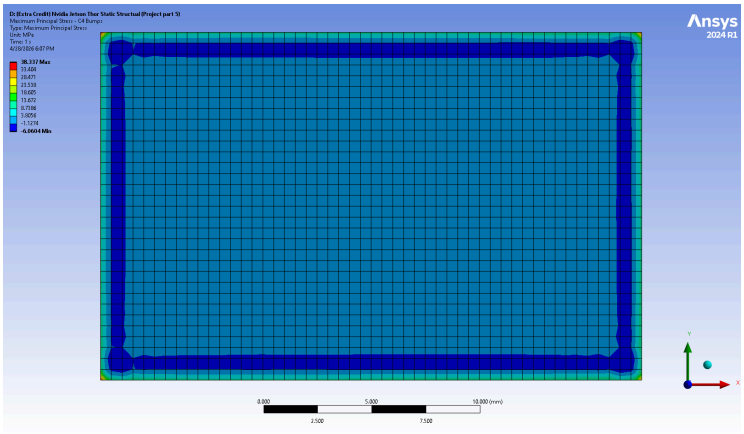
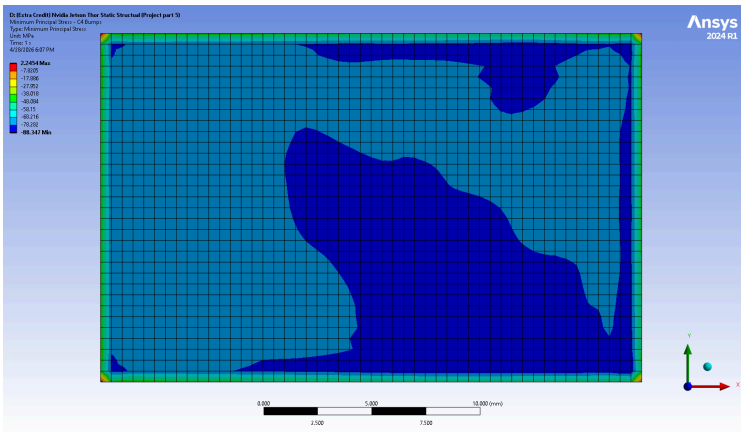
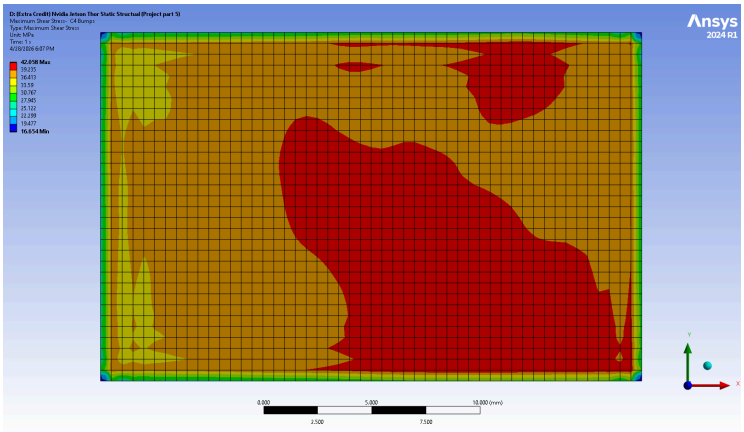
BGA	Normal σ_zz	
	Shear τ_xz	
	Shear τ_yz	

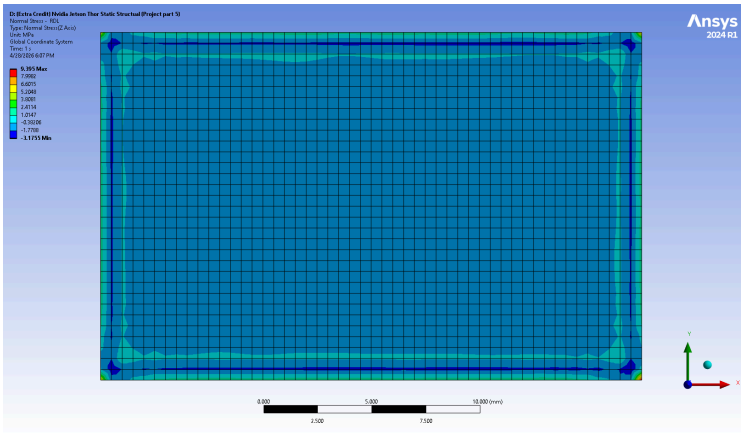
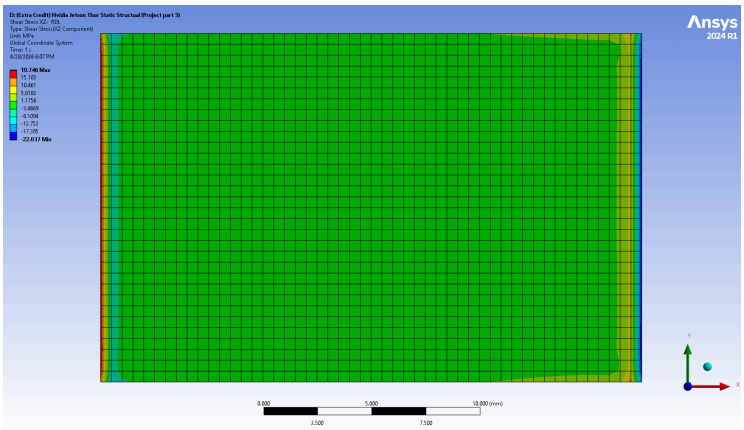
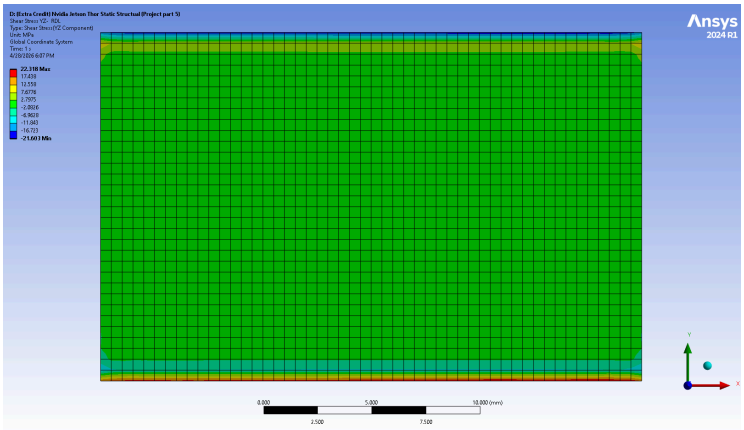
	Maximum Principal σ_1	
	Minimum Principal σ_3	
	Maximum Shear τ	

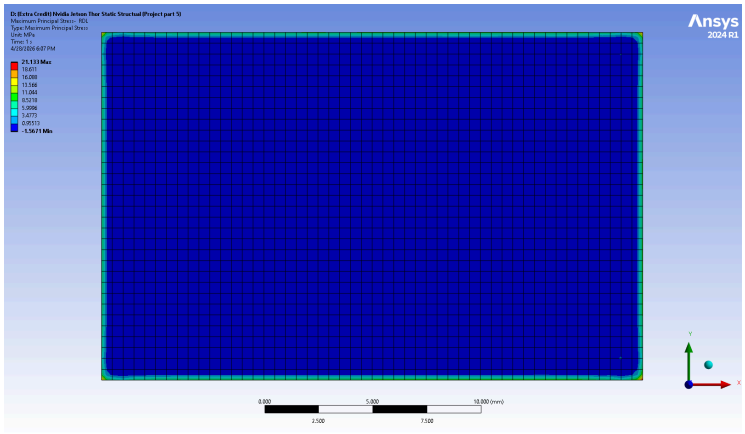
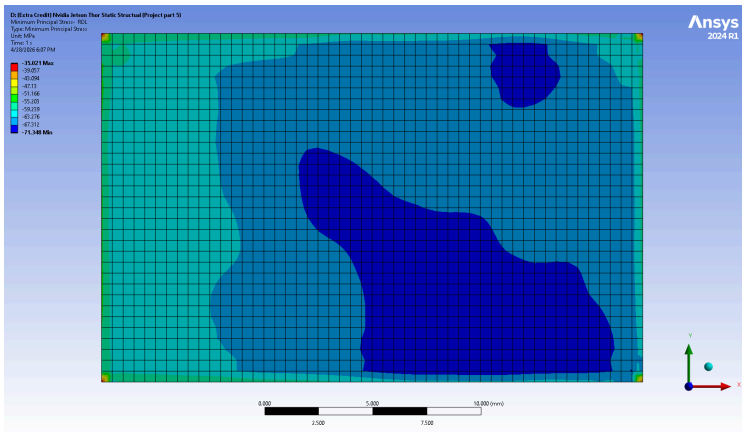
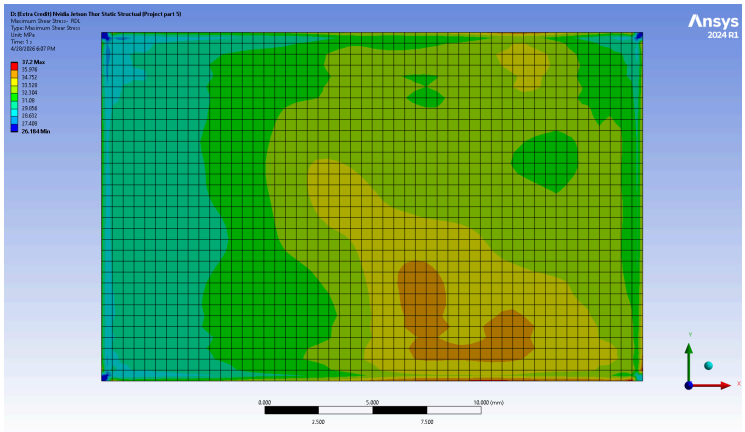
Package Substrate	Normal σ_zz	
	Shear τ_xz	
	Shear τ_yz	

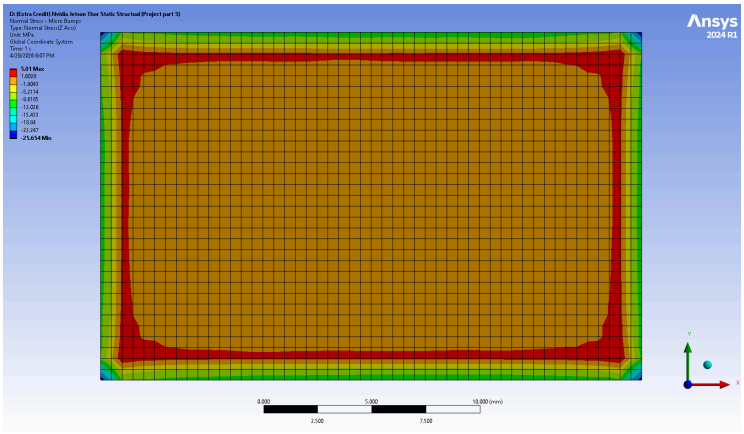
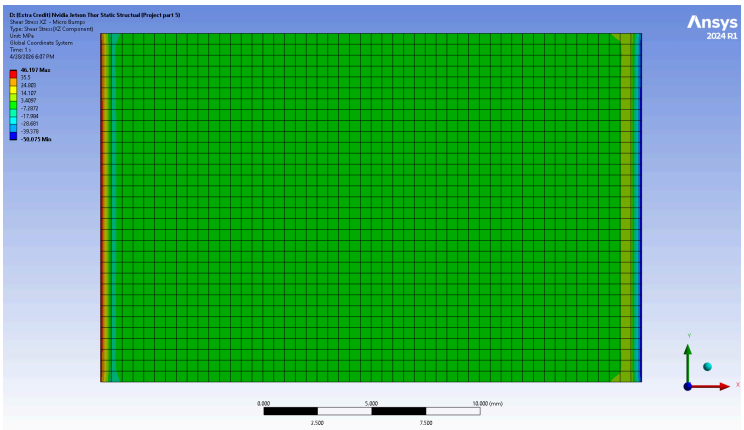
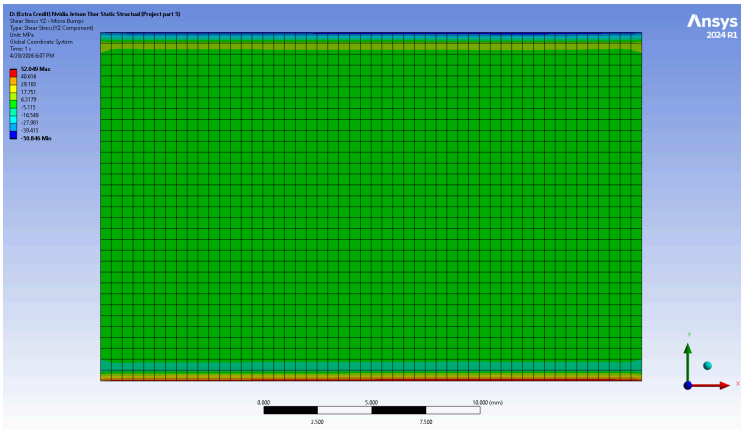
	Maximum Principal σ_1	
	Minimum Principal σ_3	
	Maximum Shear τ	

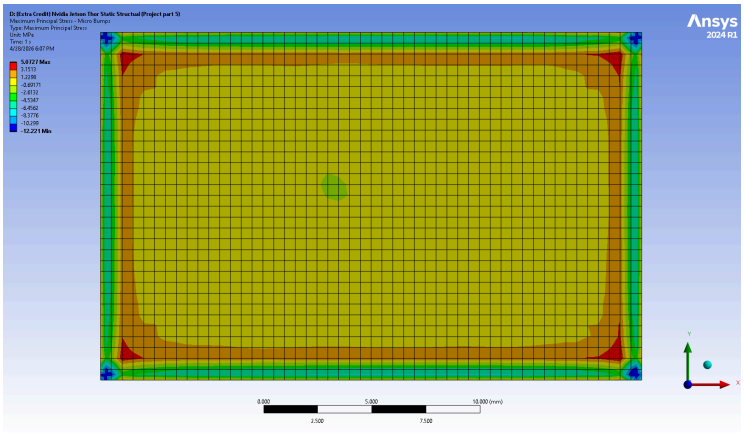
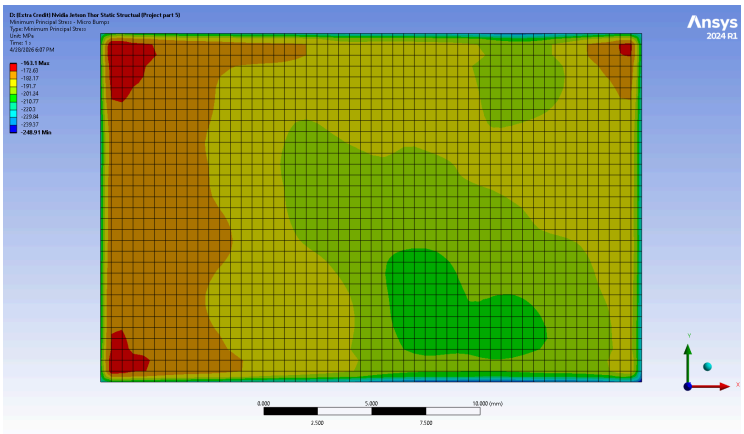
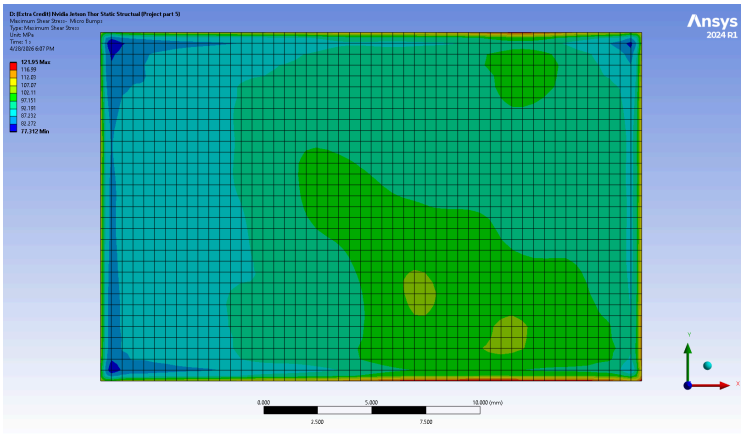
C4 Bumps	Normal σ_zz	
	Shear τ_xz	
	Shear τ_yz	

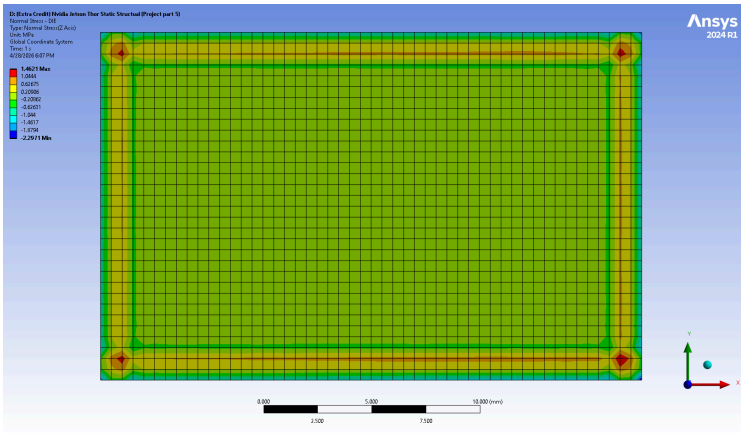
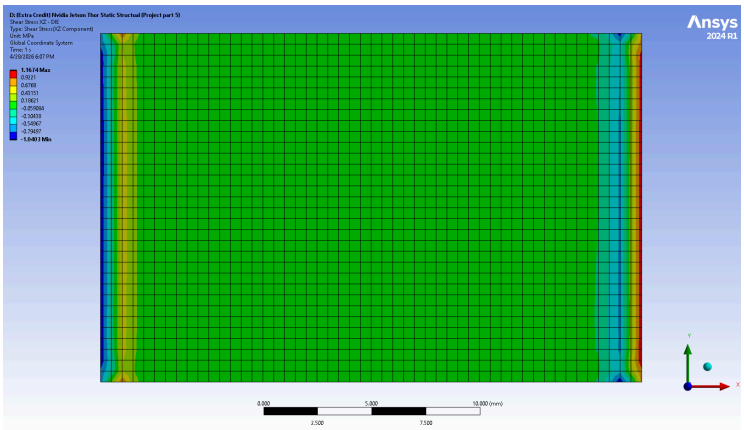
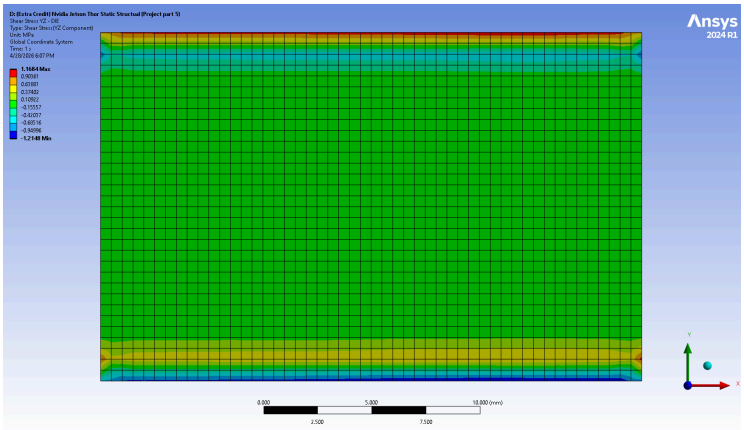
	Maximum Principal σ_1	
	Minimum Principal σ_3	
	Maximum Shear τ	

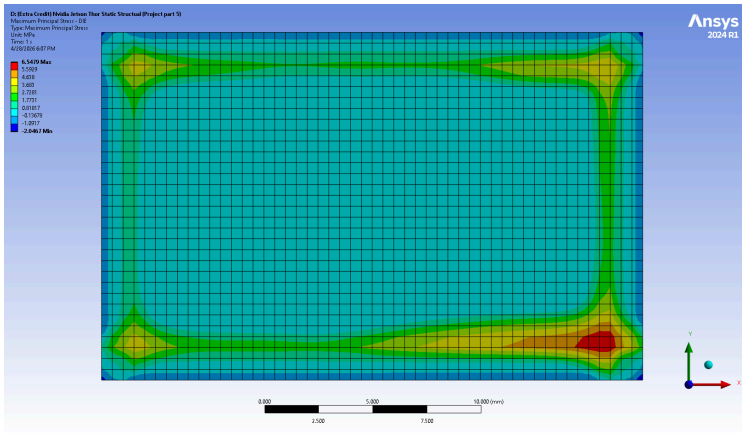
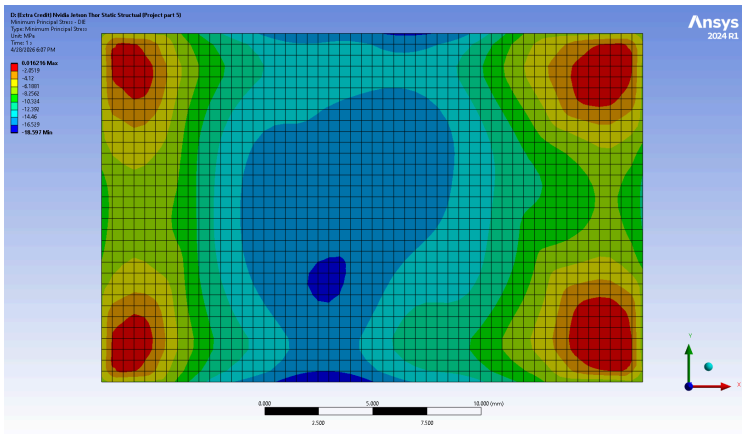
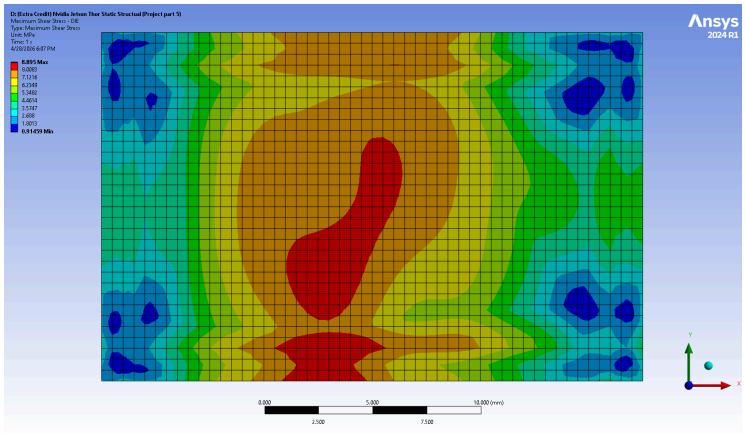
RDL	Normal σ_zz	
	Shear τ_xz	
	Shear τ_yz	

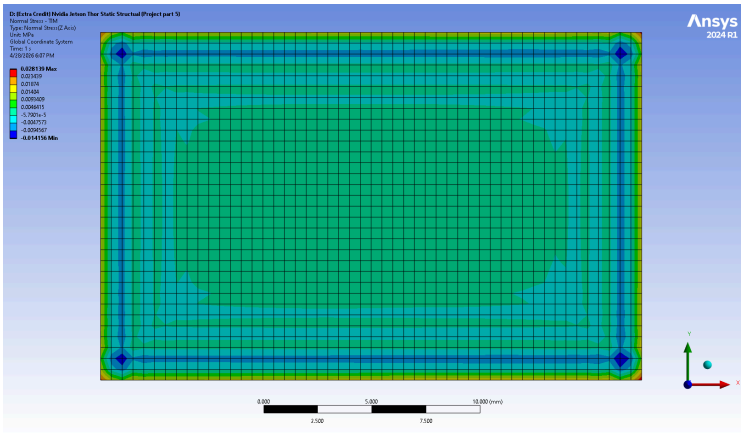
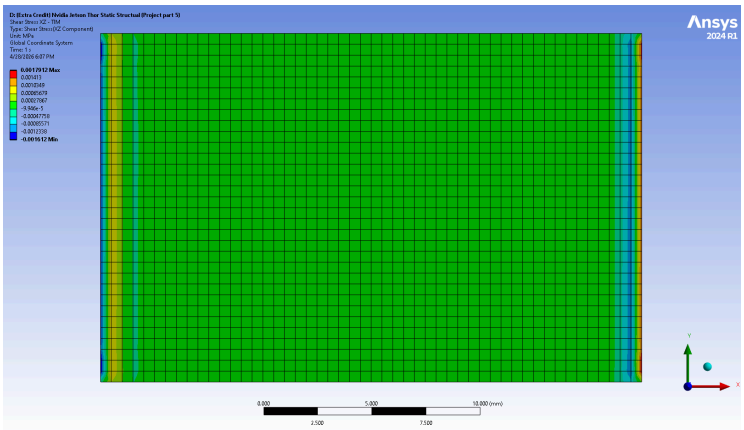
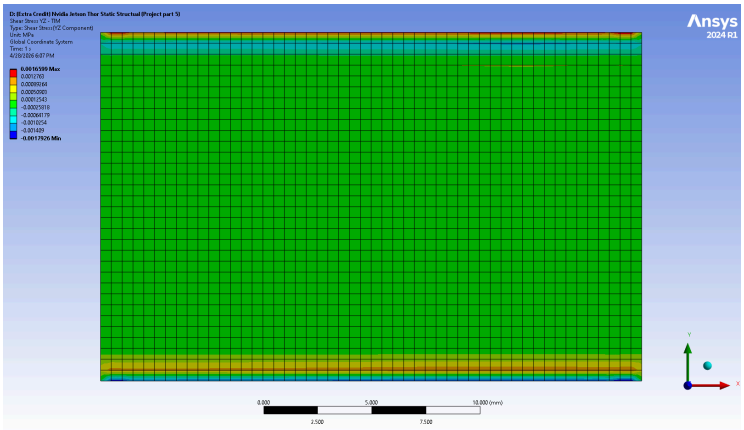
	Maximum Principal σ_1	
	Minimum Principal σ_3	
	Maximum Shear τ	

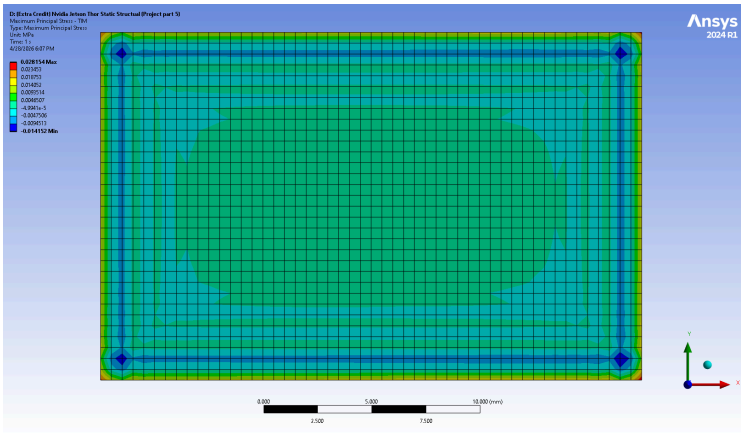
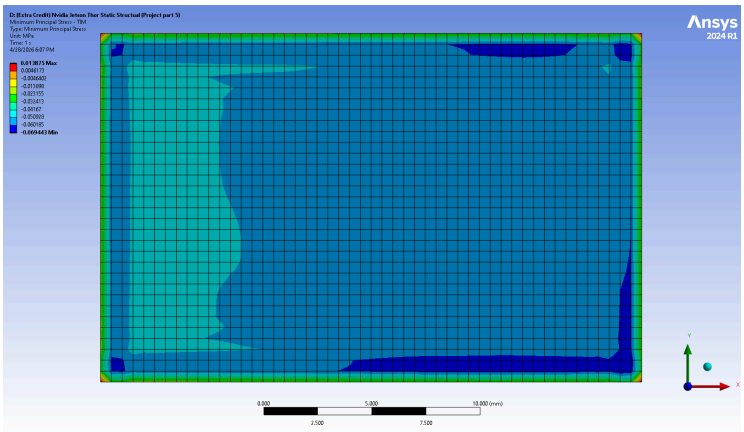
Micro Bumps	Normal σ_zz	
	Shear τ_xz	
	Shear τ_yz	

	Maximum Principal σ_1	
	Minimum Principal σ_3	
	Maximum Shear τ	

DIE	Normal σ_zz	
	Shear τ_xz	
	Shear τ_yz	

	Maximum Principal σ_1	
	Minimum Principal σ_3	
	Maximum Shear τ	

TIM	Normal σ_zz	
	Shear τ_xz	
	Shear τ_yz	

	Maximum Principal σ_1	
	Minimum Principal σ_3	
	Maximum Shear τ	